

LF14B
Schematics Document

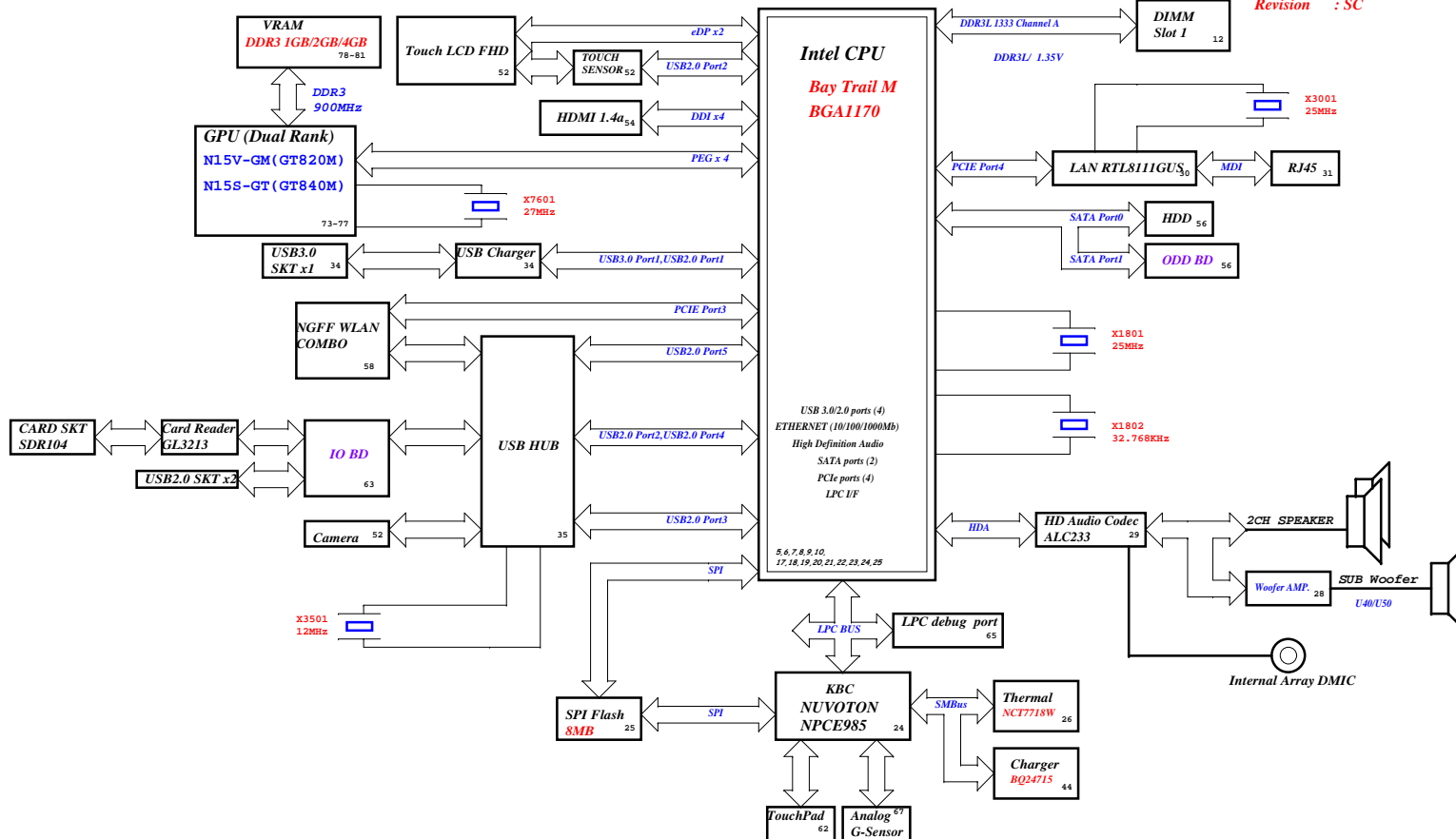
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LF14B_BT M Board Block Diagram

Project code : 4PD00U010001
PCB P/N : 13307
Revision : SC



CHARGER	
BQ24727	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
5V_S5	3D3V_S5
DCBATOUT	3D3V_S5
CPU DC/DC	
ISL95833	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
SY8208	50
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
SYSTEM DC/DC	
SY8208DQNC	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
SYSTEM LDO	
TLV70218	51
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
SYSTEM LDO	
S-1339D15	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
TLV70012	51
INPUTS	OUTPUTS
3D3V_S5	1D2V_S5
Step Down Regulator	
SYW232	51
INPUTS	OUTPUTS
1D0V_S0_P6	1D05V_S0
GPU Core	
RT8812	82
INPUTS	OUTPUTS
DCBATOUT	V6A_CORE
LOAD SWITCH	
TPS22966	37
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
LOAD SWITCH	
TPS22965	37
INPUTS	OUTPUTS
1D0V_S5	1D0V_S0
SYSTEM DC/DC	
SY8208	83
INPUTS	OUTPUTS
DCBATOUT	1D5V_V6A_S0
LOAD SWITCH	
TPS22966	83
INPUTS	OUTPUTS
1D05V_S0	1D5V_V6A_S1
3D3V_S0	3D3V_V6A_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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D

C

B

A

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SSID = CPU

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無1%排阻

reserve the 0402 0.1u caps on reset for EMI.

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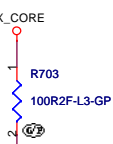
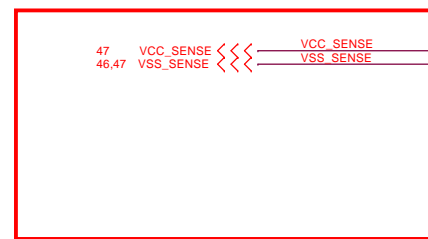
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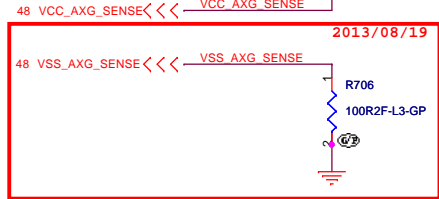
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2013/05/09



2013/08/19



CPU1G

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CORE_VCC_SENSE_P28
UNCORE_VNN_SENSE_BB8
CORE_VSS_SENSE_N28

BAY TRAIL-M/D SOC

DRAM_VDD_S4_BD49
DRAM_VDD_S4_BD52
DRAM_VDD_S4_BD53
DRAM_VDD_S4_BF44
DRAM_VDD_S4_BF45
DRAM_VDD_S4_BJ48
DRAM_VDD_S4_C51
DRAM_VDD_S4_D44
DRAM_VDD_S4_F49
DRAM_VDD_S4_F52
DRAM_VDD_S4_F53
DRAM_VDD_S4_H46
DRAM_VDD_S4_M41
DRAM_VDD_S4_M42
DRAM_VDD_S4_V38
DRAM_VDD_S4_Y38

VDDQ_CPU

AA27 CORE_VCC_S0IX_AA27
AA29 CORE_VCC_S0IX_AA29
AA30 CORE_VCC_S0IX_AA30
AC27 CORE_VCC_S0IX_AC27
AC29 CORE_VCC_S0IX_AC29
AC30 CORE_VCC_S0IX_AC30
AD27 CORE_VCC_S0IX_AD27
AD29 CORE_VCC_S0IX_AD29
AD30 CORE_VCC_S0IX_AD30
AF27 CORE_VCC_S0IX_AF27
AF29 CORE_VCC_S0IX_AF29
AG27 CORE_VCC_S0IX_AG27
AG29 CORE_VCC_S0IX_AG29
AG30 CORE_VCC_S0IX_AG30
P26 CORE_VCC_S0IX_P26
P27 CORE_VCC_S0IX_P27
U27 CORE_VCC_S0IX_U27
U29 CORE_VCC_S0IX_U29
V27 CORE_VCC_S0IX_V27
V29 CORE_VCC_S0IX_V29
V30 CORE_VCC_S0IX_V30
Y27 CORE_VCC_S0IX_Y27
Y29 CORE_VCC_S0IX_Y29
Y30 CORE_VCC_S0IX_Y30

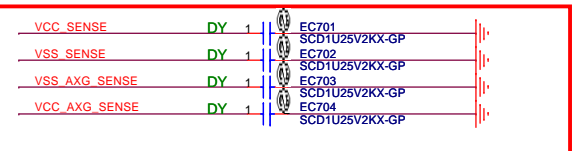
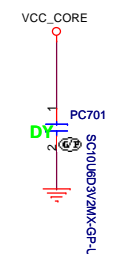
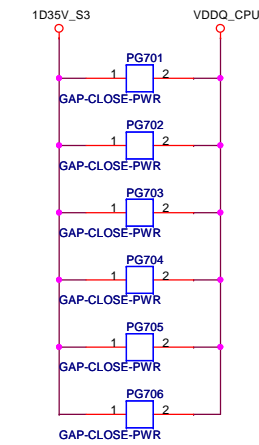
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UNCORE_VNN_S3_AC22
UNCORE_VNN_S3_AC24
UNCORE_VNN_S3_AD22
UNCORE_VNN_S3_AD24
UNCORE_VNN_S3_AF22
UNCORE_VNN_S3_AF24
UNCORE_VNN_S3_AG22
UNCORE_VNN_S3_AG24
UNCORE_VNN_S3_AJ22
UNCORE_VNN_S3_AJ24
UNCORE_VNN_S3_AK22
UNCORE_VNN_S3_AK24
UNCORE_VNN_S3_AK25
UNCORE_VNN_S3_AK27
UNCORE_VNN_S3_AK29
UNCORE_VNN_S3_AK30
UNCORE_VNN_S3_AK32
UNCORE_VNN_S3_AM22

AA24
AC22
AC24
AD22
AD24
AF22
AF24
AG22
AG24
AJ22
AJ24
AK22
AK24
AK25
AK27
AK29
AK30
AK32
AM22

TP_CORE_V1P05_S4

TP2_CORE_VCC_S0IX

BAY-TRAIL-GP



reserve the 0402 0.1u caps on reset for EMI.

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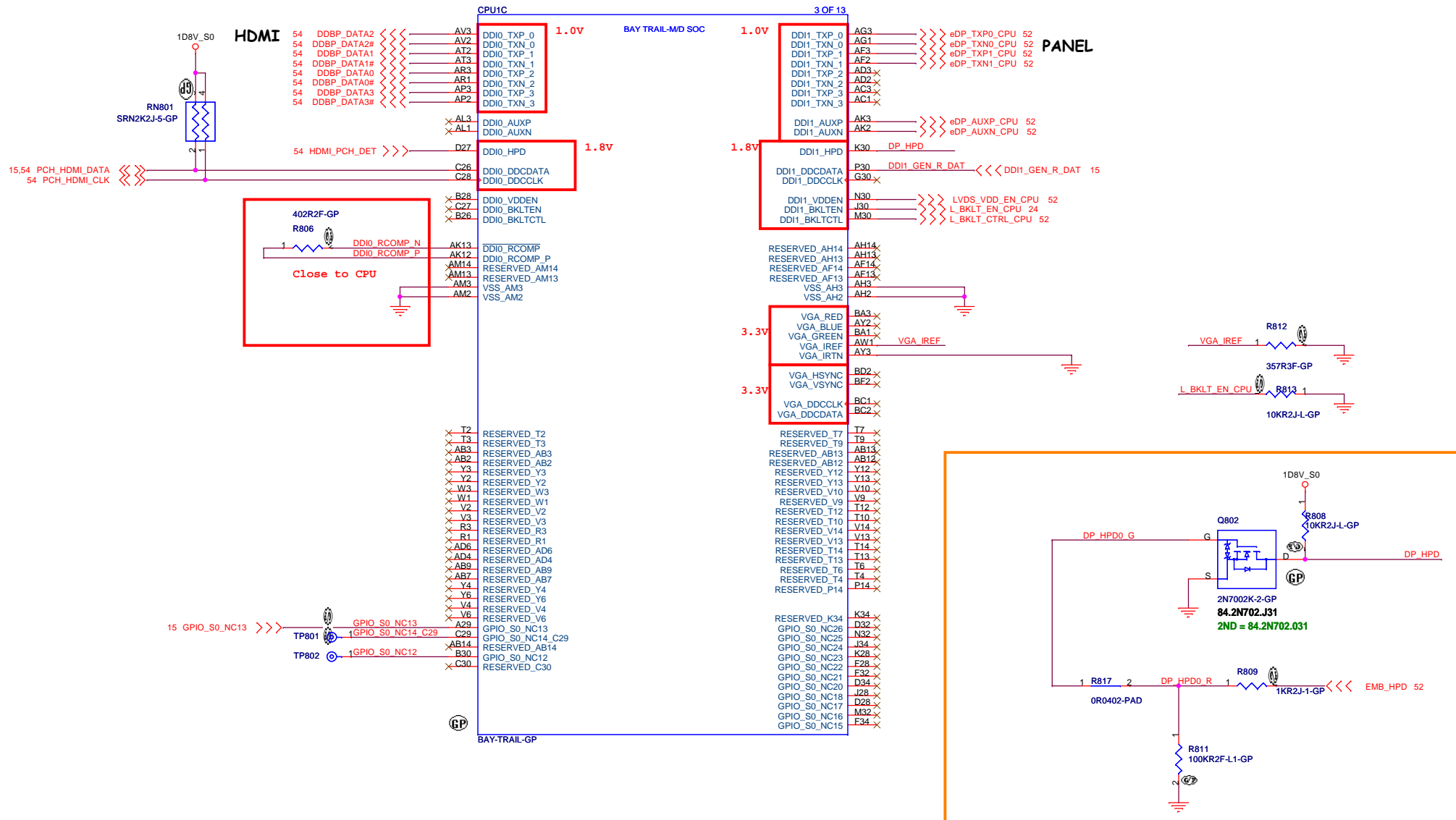
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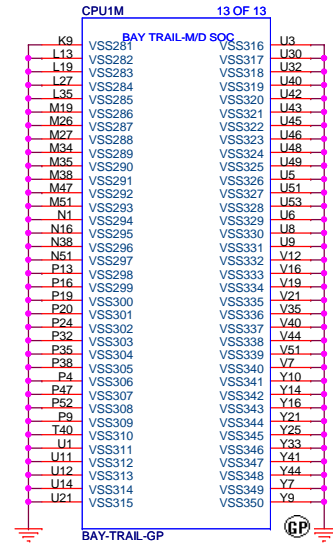
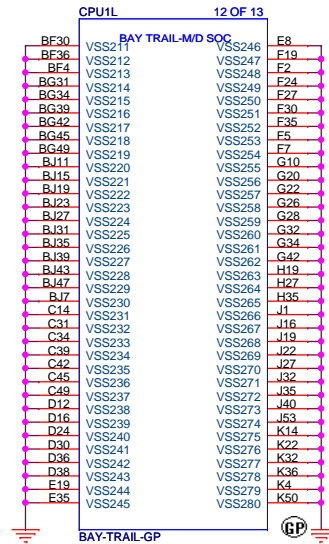
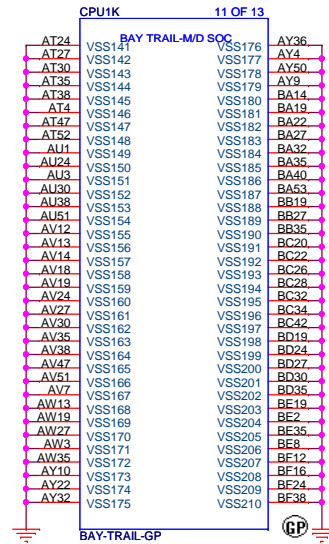
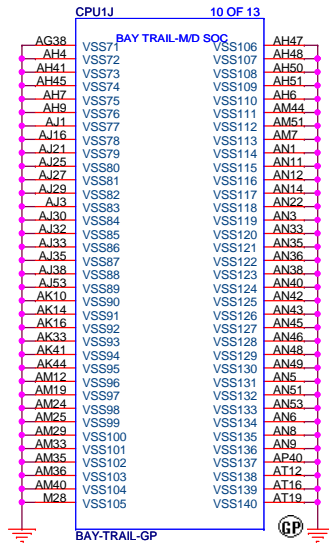
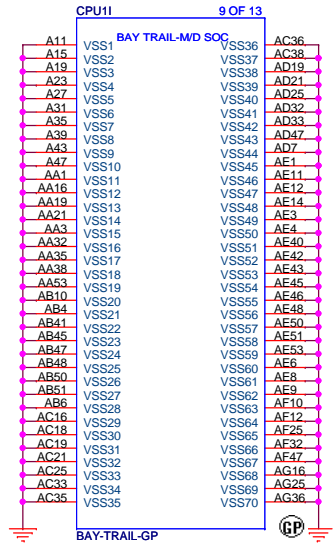


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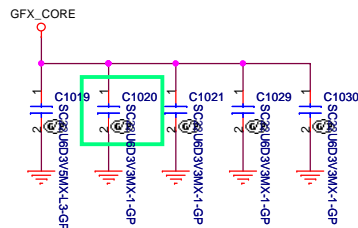
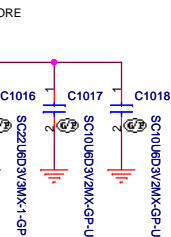
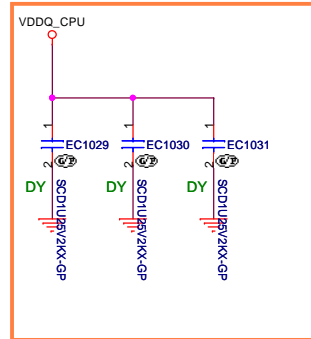
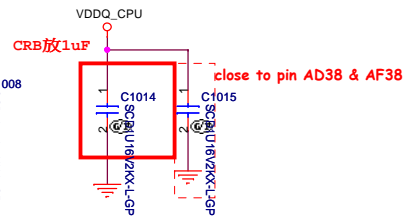
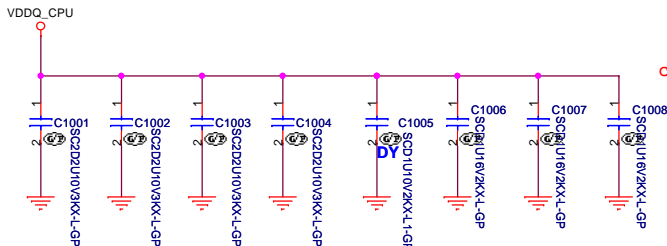
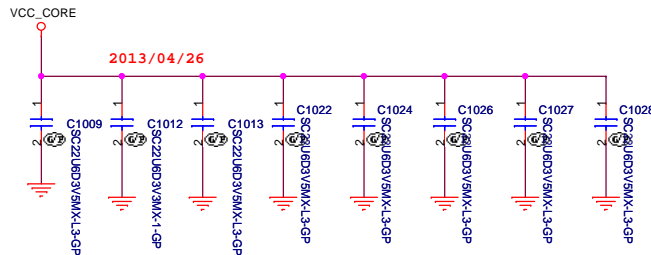
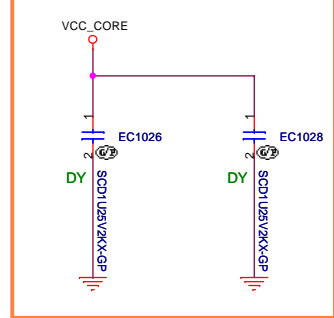
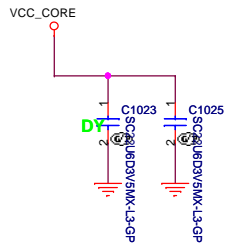
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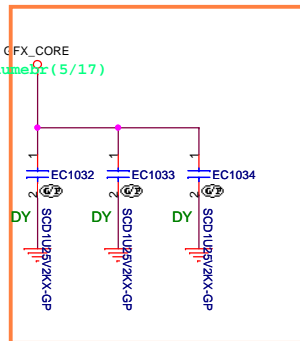
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reserve the 0402 0.1u caps on reset for EMI(5/9).

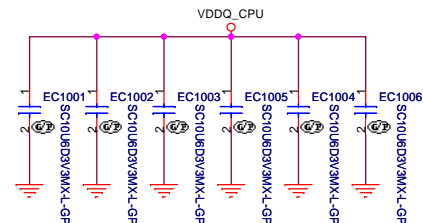


Change part number (5/17)



reserve the 0402 0.1u caps on reset for EMI(5/9).

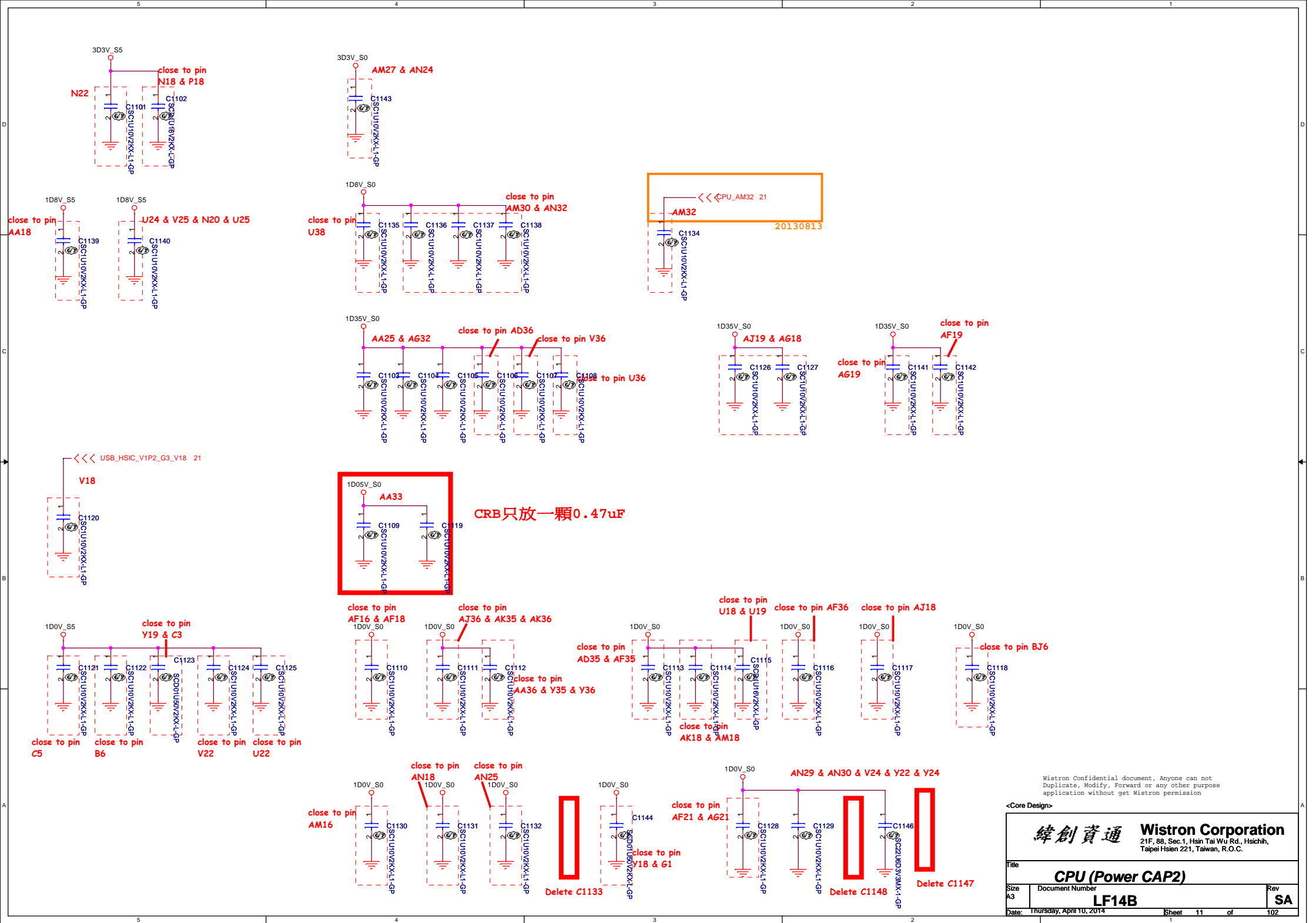
reserve the 0402 0.1u caps on reset for EMI(5/9).



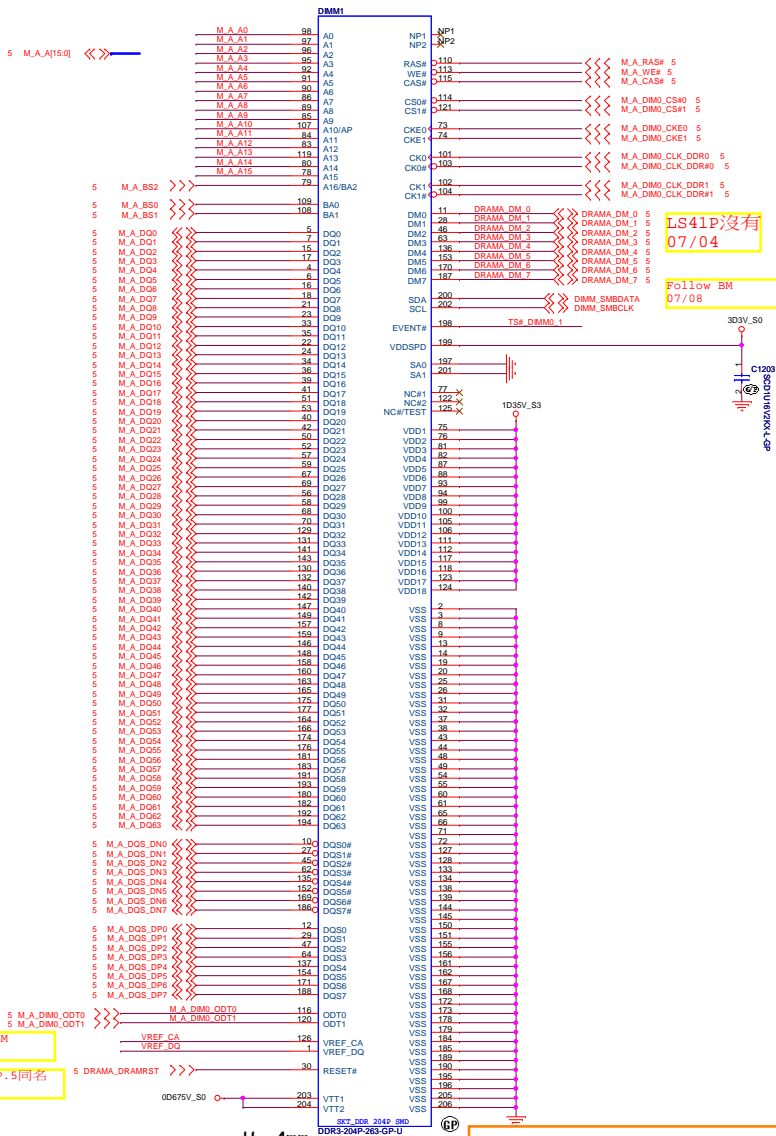
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SSID = MEMORY



5	4	3	2	1
D				D
C				C
B				B
A				A

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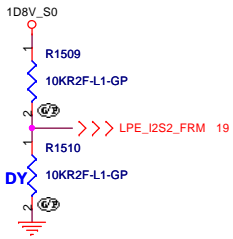
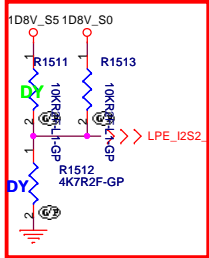
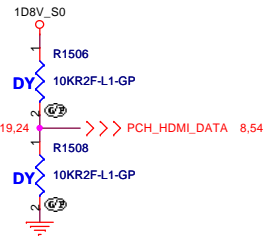
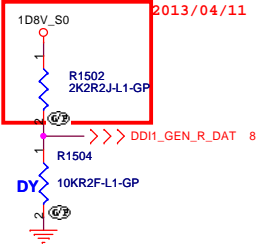
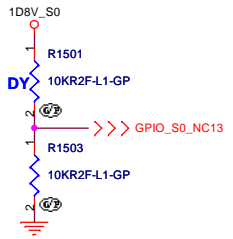
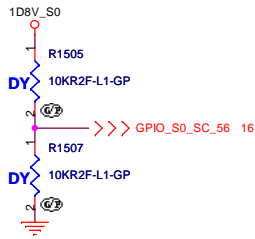
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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	DDI0 detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDI0 not detected	DDI1 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

30.2 LPE_I2S2_DATAOUT/ GPIO_S0_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO_S0_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

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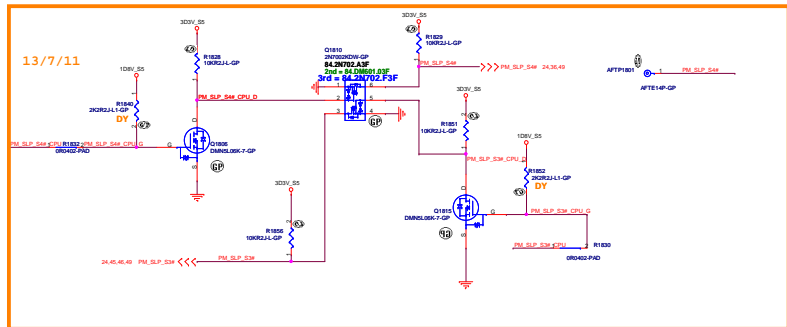
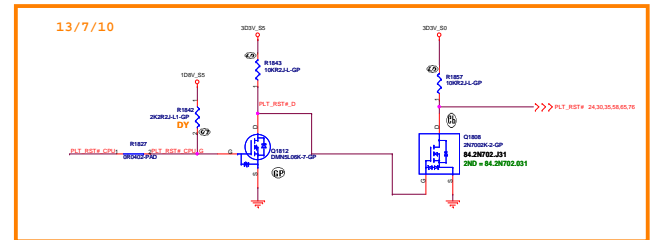
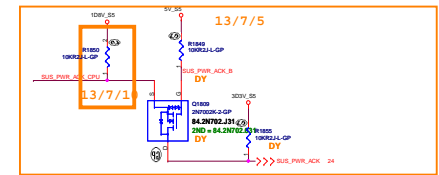
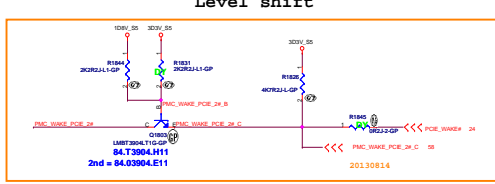
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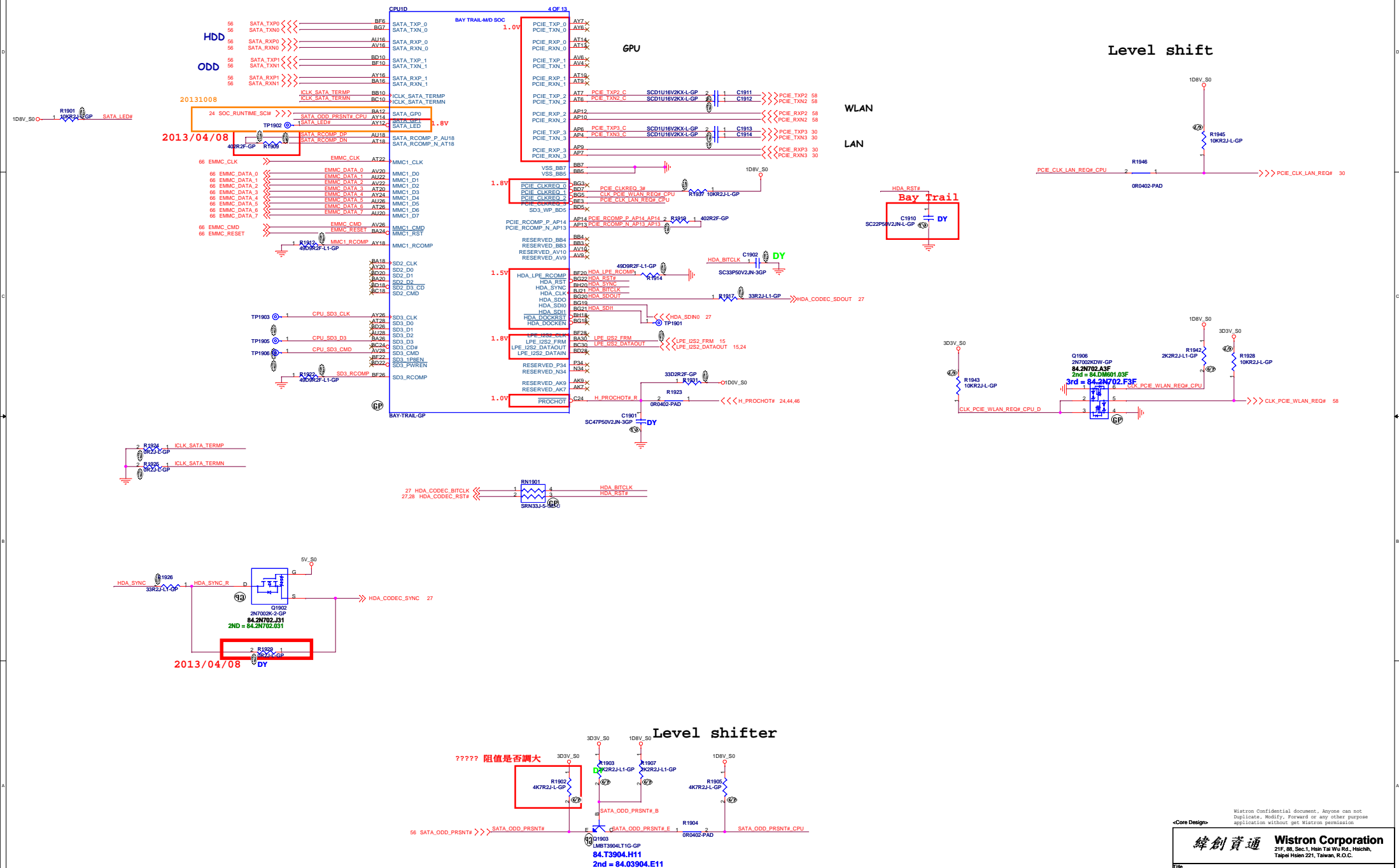
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Level shift



reserve the 0402 0.1u caps on reset for EMI(5/9).

SSID = PCH



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SSID = PCH

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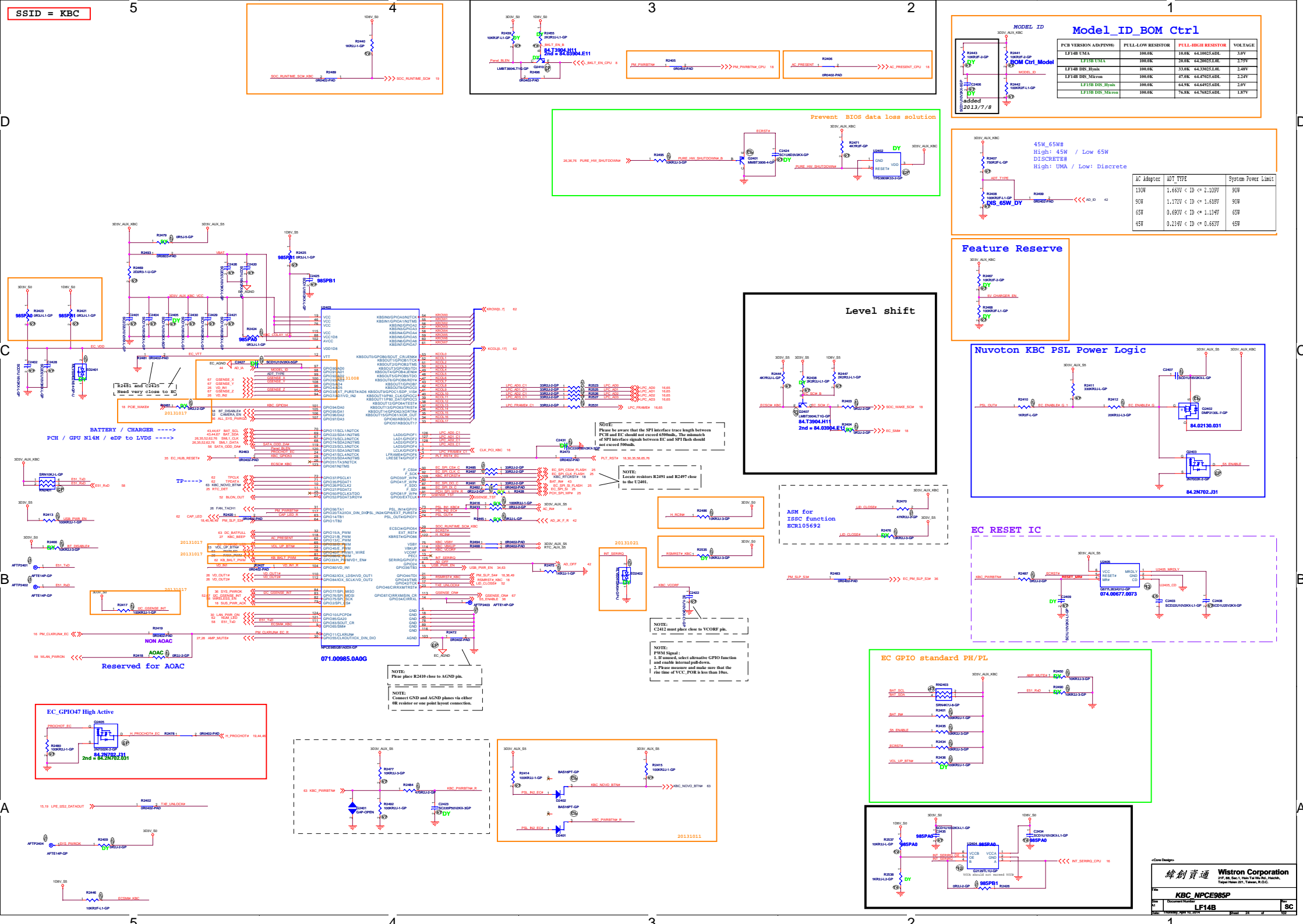
SSID = PCH

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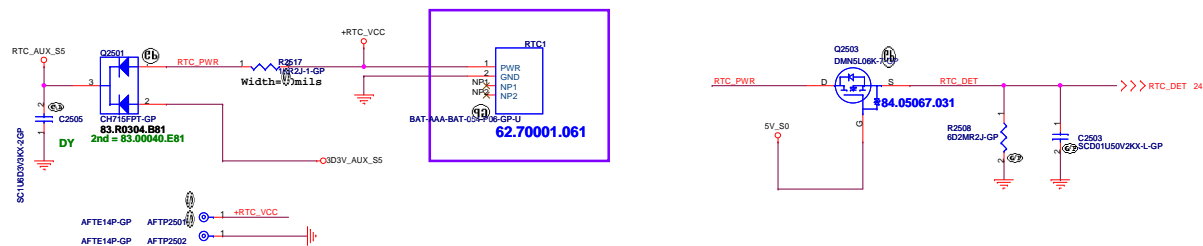
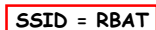
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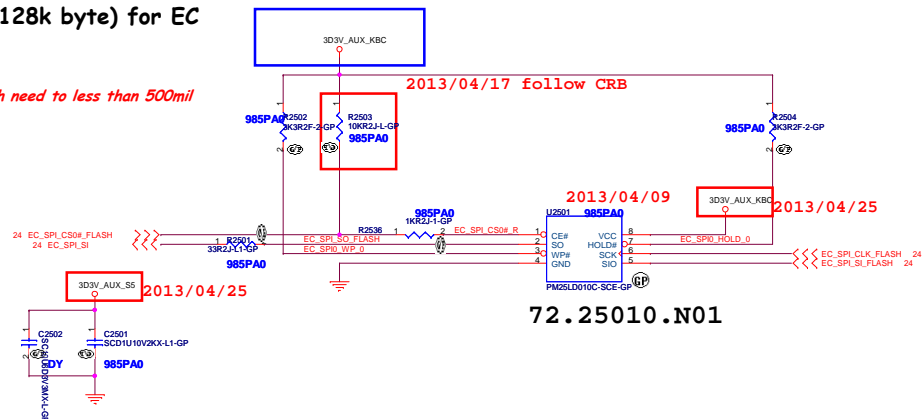


SPI FLASH ROM (8M byte) for PCH

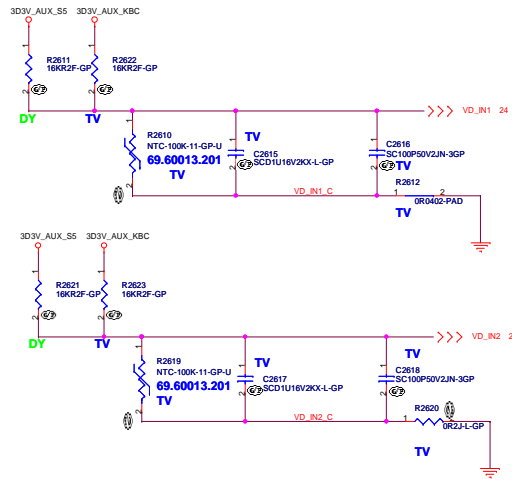
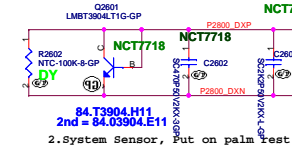


Copy from Lily LS41P 2013/7/8
Need to Check if needed !!
If needed, need to find a GPIO
Pin on CPU side and connect it.

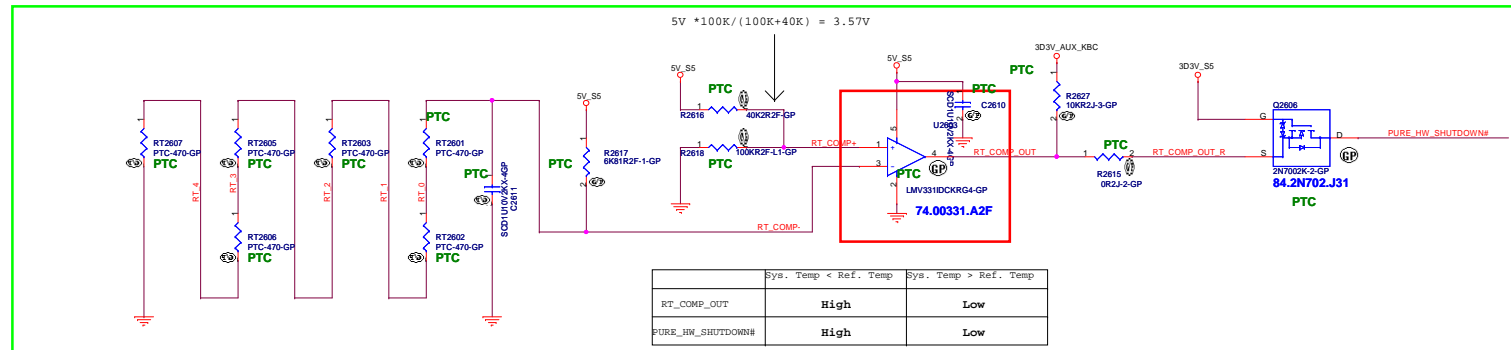
SPI FLASH ROM (128k byte) for EC



Thermal sensor NCT 7718W



PTC Function M40/M50 (All Series Reserved)



	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

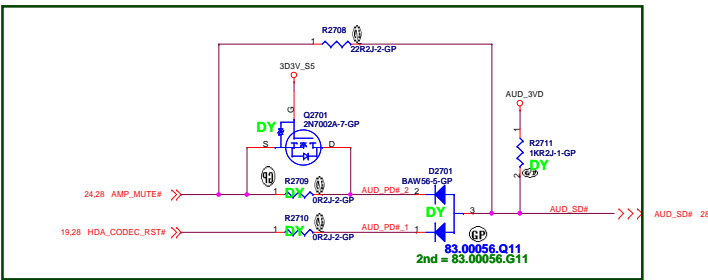
[illegible]

	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5					
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

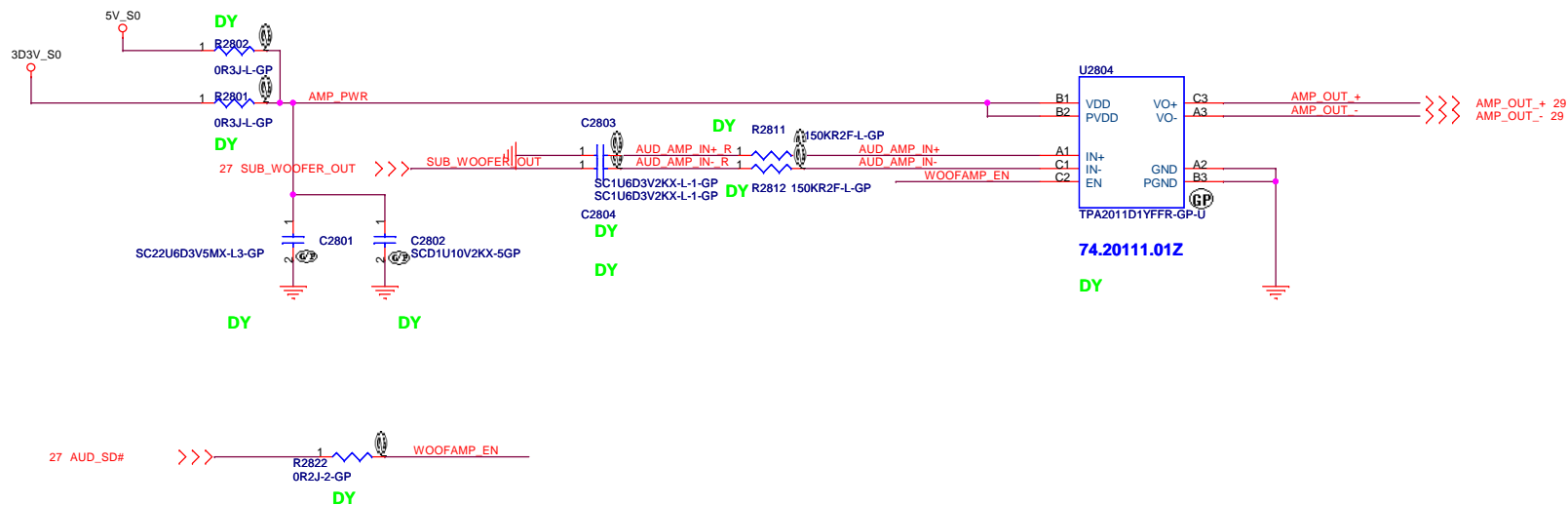
	PTC Position
RT2606	5V_PWR_DC/DC_High_side_FET (PU4507)
RT2605	3V_PWR_DC/DC_High_side_FET (PU4504)
RT2609	Bt+ High_side_FET (PU4403)
RT2607	1D05V_PWR_DC/DC_High_side_FET (PU4802)
RT2603	1D35V_S3_DC/DC_High_side_FET (PU4902)
RT2610	1D5V_PWR_VGA_DC/DC_High_side_FET(PU5110)
RT2602	VCC_CORE_Driver-1 (PU4702)
RT2601	VCC_CORE_Driver-2 (PU4701)
RT2608	VGA_CORE_DC/DC_MOSFET (PU8202)

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Title			
Thermal 7718/Fan Controllor P2793			
Size	Document Number	Rev	
A2	LF14B	SC	
Date:	Thursday, April 10, 2014	Sheet	26 of 102

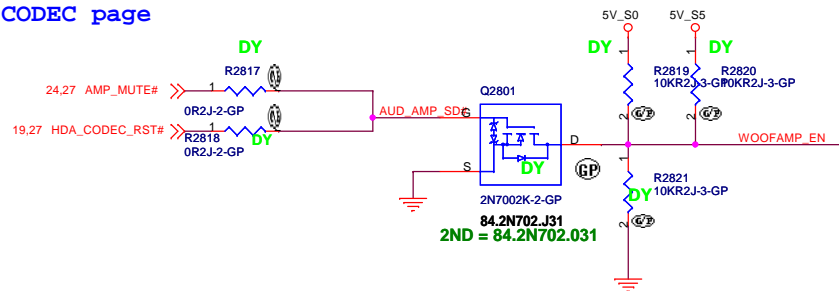


WOOFER AMP. U40/U50



Reference LZ57 AMP Design (Reserved)

Also Reserved Direct control from AMP_MUTE# SB 0923'10
in CODEC page



<Core Design>

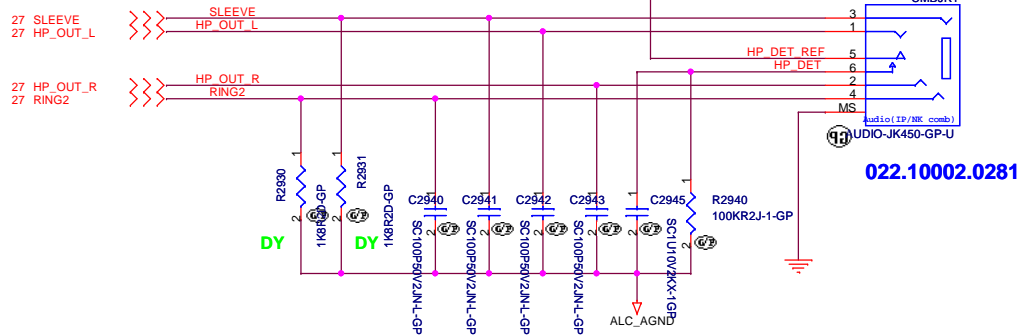
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			Audio AMP	
Size	Document Number	Rev		SA
A3	LF14B			
Date:	Thursday, April 10, 2014	Sheet	28	of 102

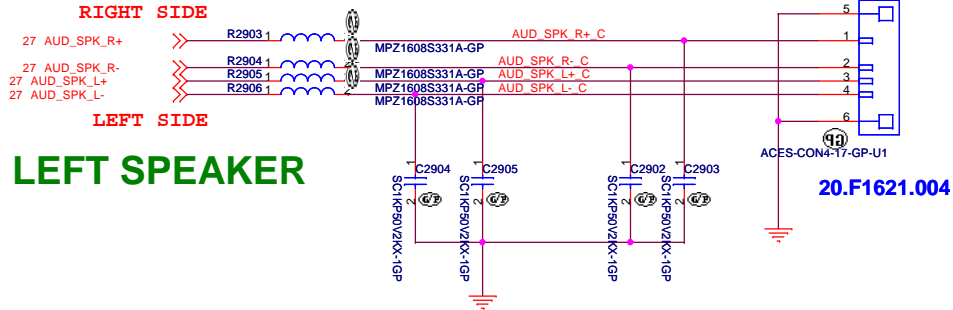
Wait to update P/N

COMBO JACK

2013/9/22 Add HP_DET# RC

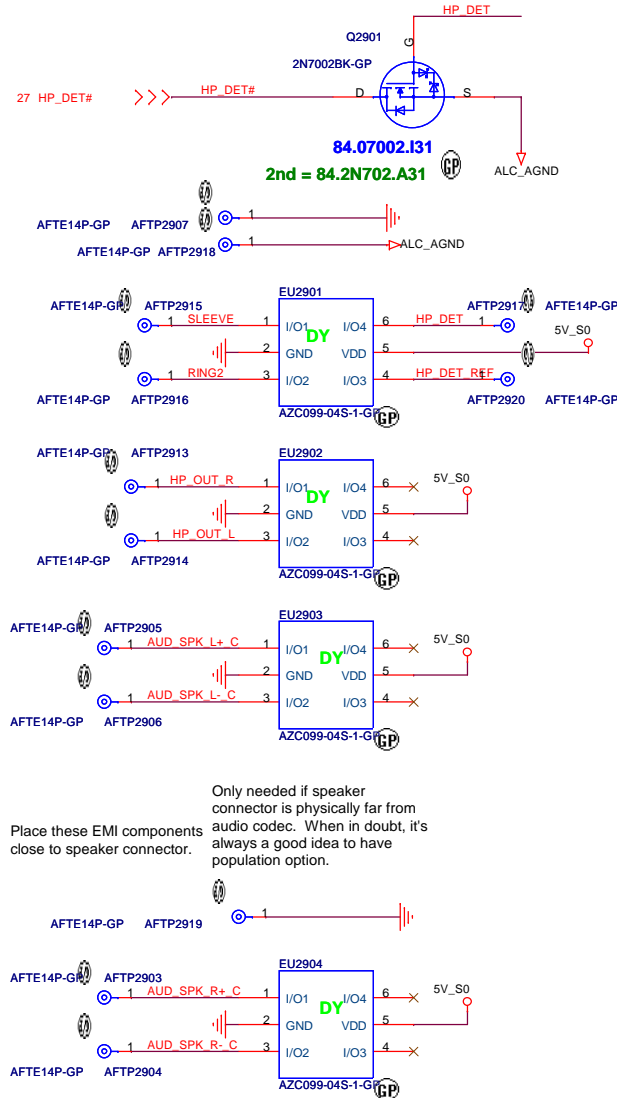
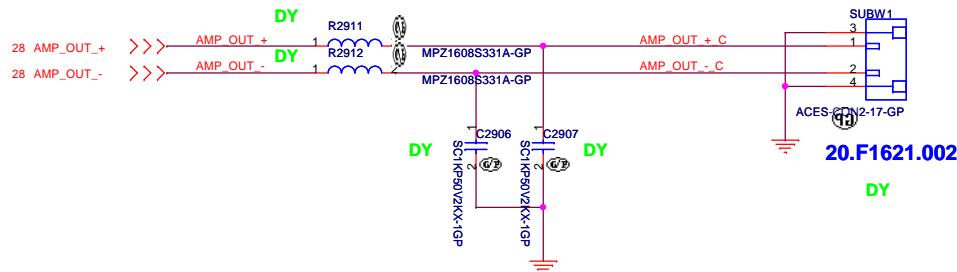


RIGHT SPEAKER

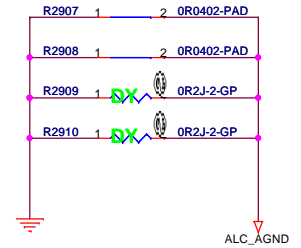
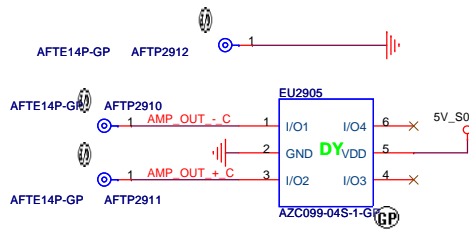
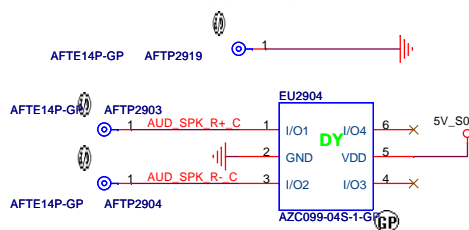


LEFT SPEAKER

SUB WOOFER (U40/U50)



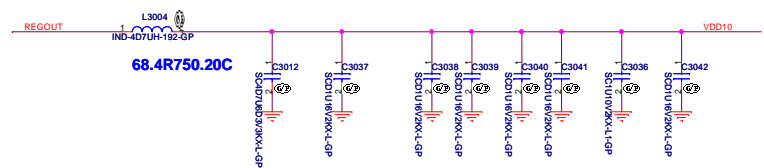
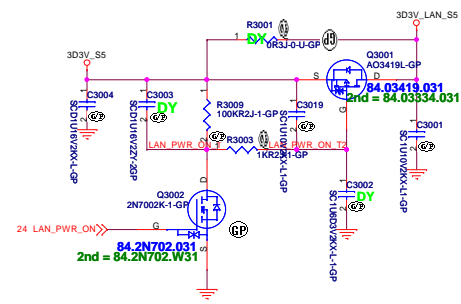
Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.



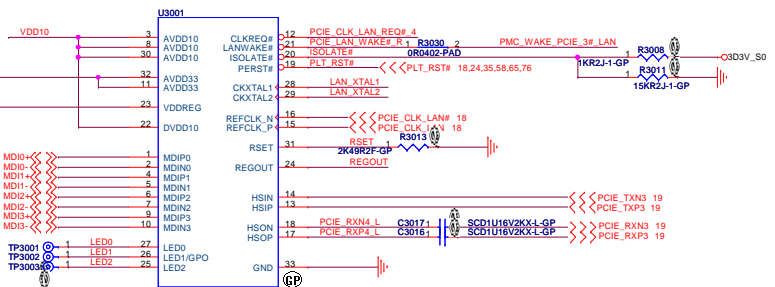
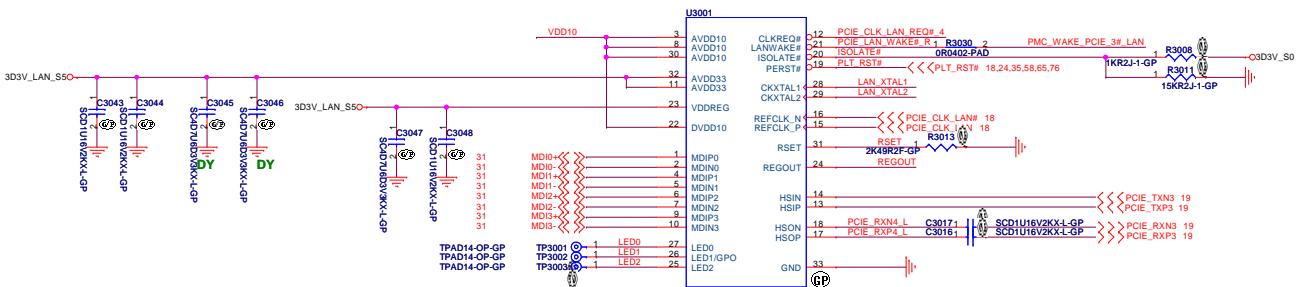
<Core Design>

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Title		MIC/SPEAKER/AUDIO JACK	
Size	Custom	Document Number	Rev
Date: Thursday, April 10, 2014		LF14B	SC
Sheet 29 of 102			

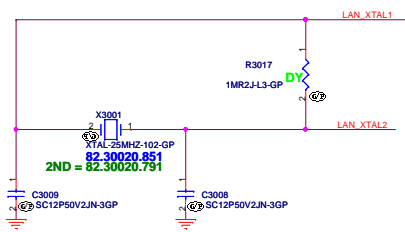


For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
 *Place C3038 to C3041 close to each VDD10 pin-- 3, 8, 22, 30
 For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
 *Place C20 and C21 close to each VDD10 pin-- 22 (Reserved)

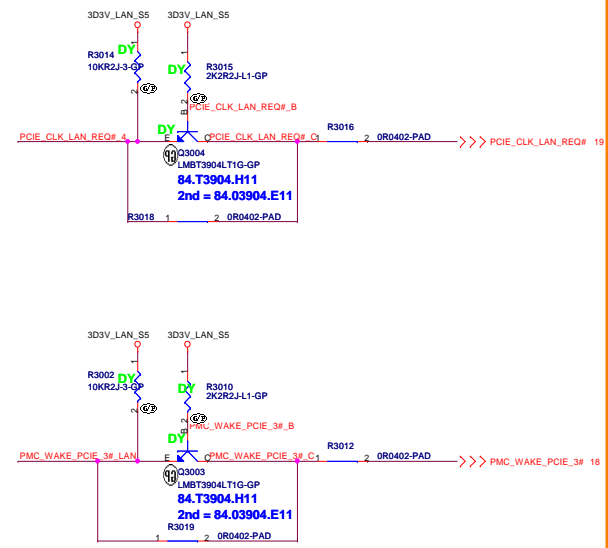


RTL8111GUS-CG-GP-U1
 71.08111.W03
 10/100 = 71.08106.003
 GIGA = 71.08111.W03

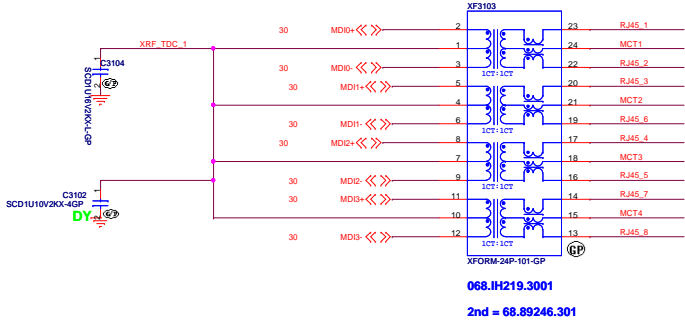
25MHz XTAL



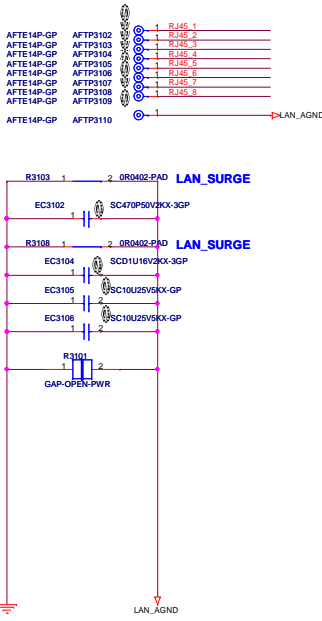
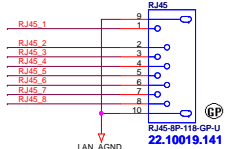
Level shifter



10/100M/1000M Lan Transformer

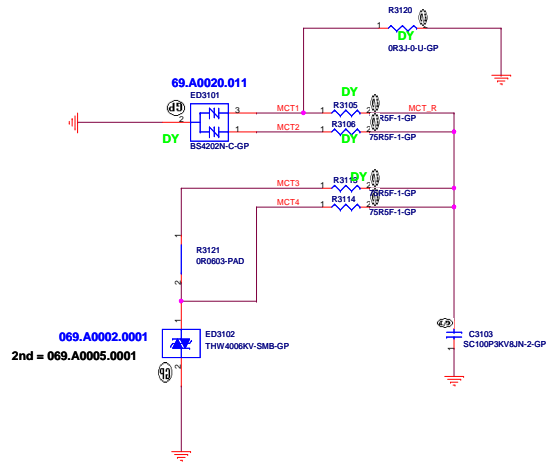
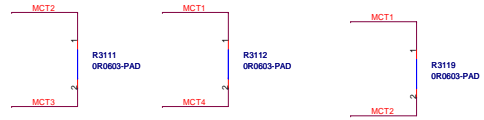


LAN Connector



10/100/1000 LAN surge circuit

For test stuff



Blanking

<Core Design>

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Title GL834L(CARD READER)			
Size Custom	Document Number LF14B		Rev SC
Date:	Tuesday, October 22, 2013	Sheet	32 of 102

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>CARD Reader</div>	
Size <div>A4</div>	Document Number <div>LF14B</div>
Date <div>Tuesday, October 22, 2013</div>	Rev <div>SC</div>
Date <div>Tuesday, October 22, 2013</div> Sheet <div>33</div> of <div>102</div>	

Non USB Charger (U40/U50)

2013/8/30 update
Reserved for option

USB3.0 Port1

Support 2A

at least 80 mil

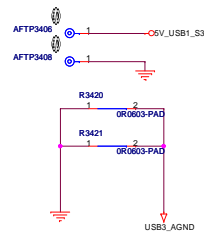
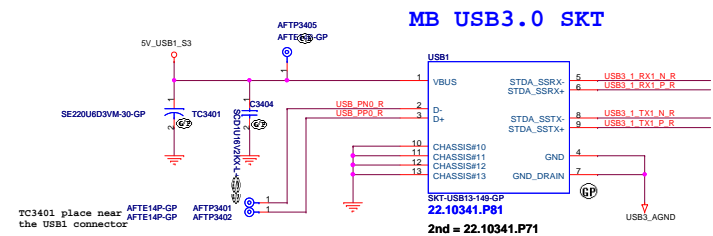
at least 80 mil

16.39 USB_P0D <<< USB_P0D 2 R3403 1 USB_P0D_CHG_R 2 R3409 1 USB_P0D_CHG

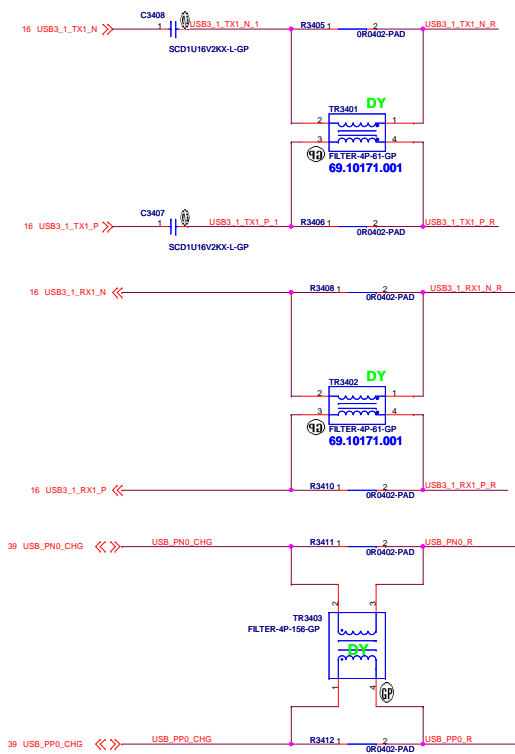
16.39 USB_P0D <<< USB_P0D 2 R3403 1 USB_P0D_CHG_R 2 R3409 1 USB_P0D_CHG

16.39 USB_PP0 <<< USB_PP0 2 R3404 1 USB_PP0_CHG_R 2 R3407 1 USB_PP0_CHG

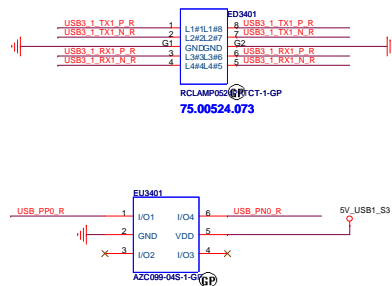
16.39 USB_PP0 <<< USB_PP0 2 R3404 1 USB_PP0_CHG_R 2 R3407 1 USB_PP0_CHG



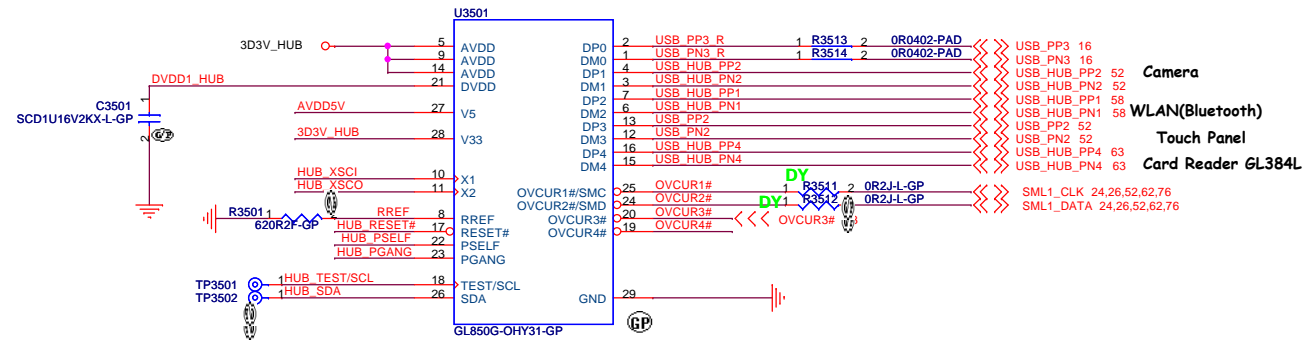
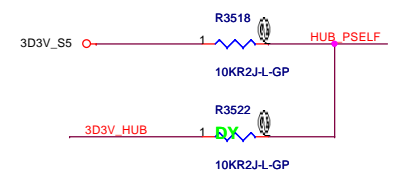
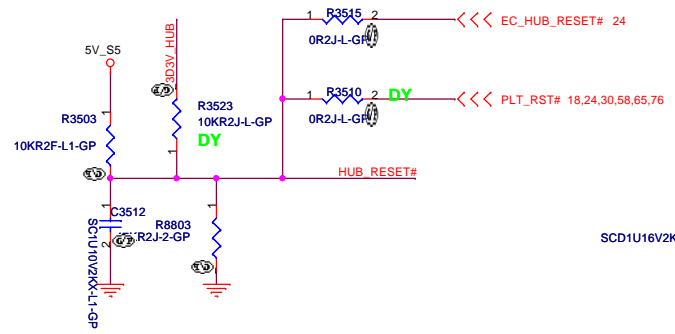
MB USB3.0 SKT



ESD circuit



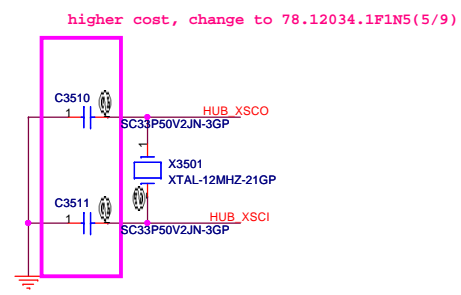
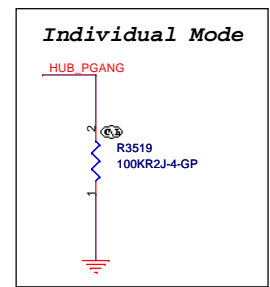
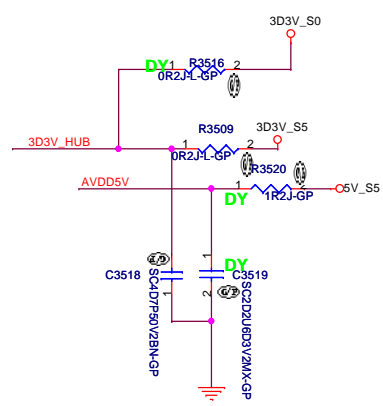
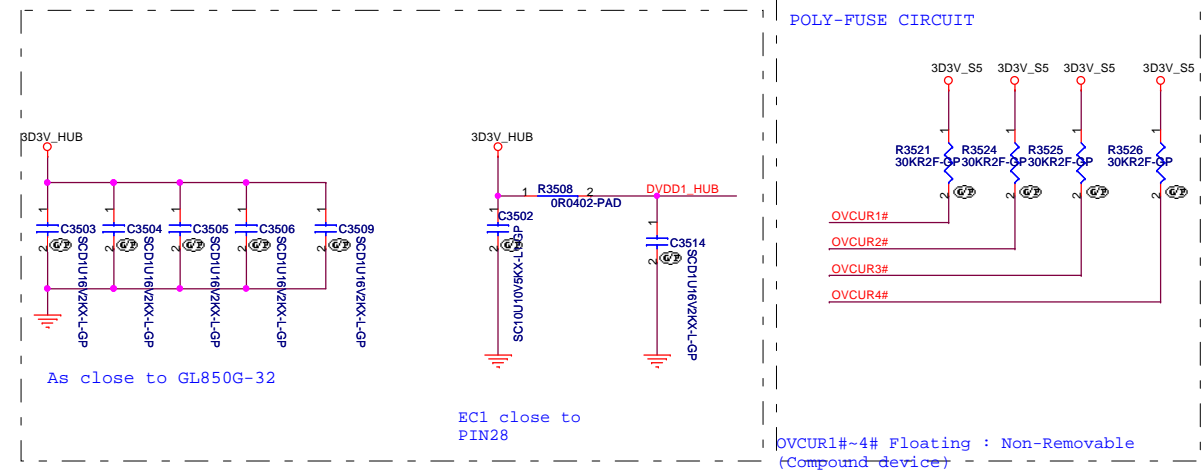
13/07/14
Del R3507



USB Table

Pair	Device
1	CCD
2	WLAN(Bluetooth)
3	USB 2.0
4	Cardreader

Camera
WLAN(Bluetooth)
Touch Panel
Card Reader GL384L



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Title: **USB HUB**

Size: Custom Document Number: **LF14B** Rev: SA

Date: Thursday, April 10, 2014 Sheet 35 of 102

Power Sequence

Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					

DDR3_VCCA_PWRGD

DDR3_DRAM_PWROK

From EC

Delay 104ms with ALL_SYS_PWROK

ALL_SYS_PWRGD

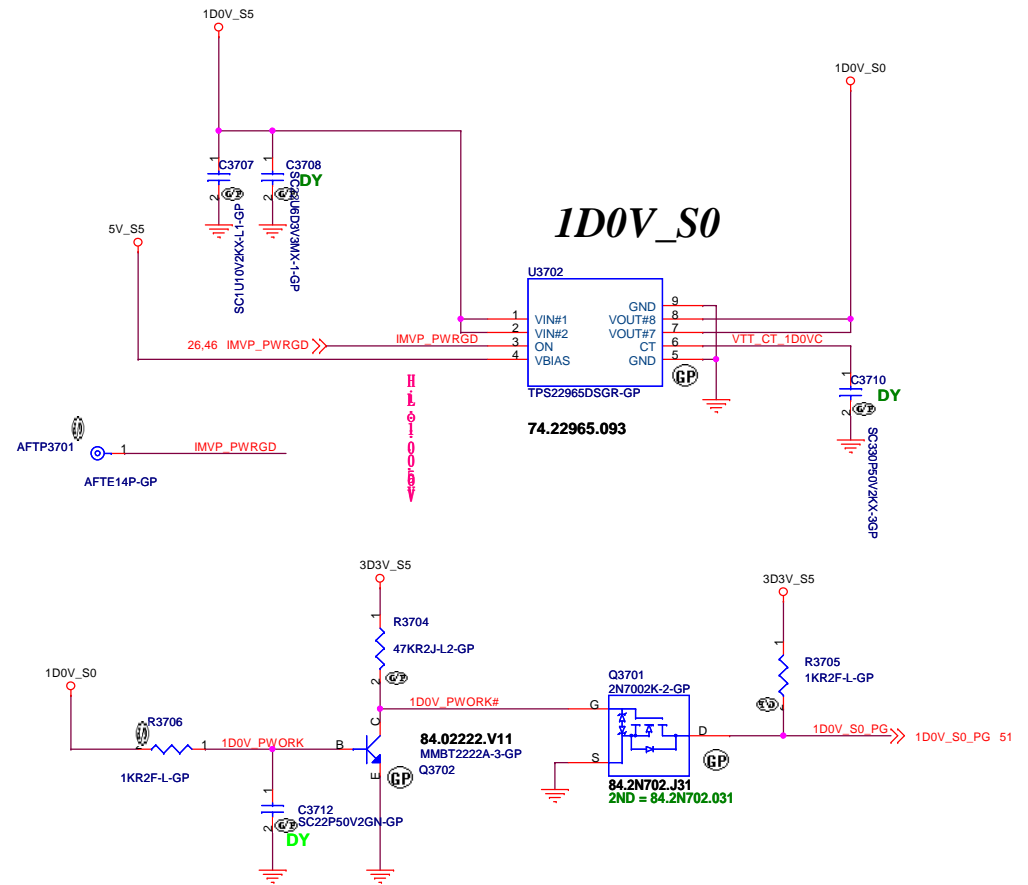
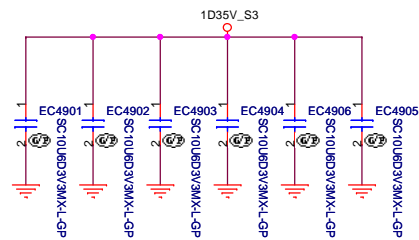
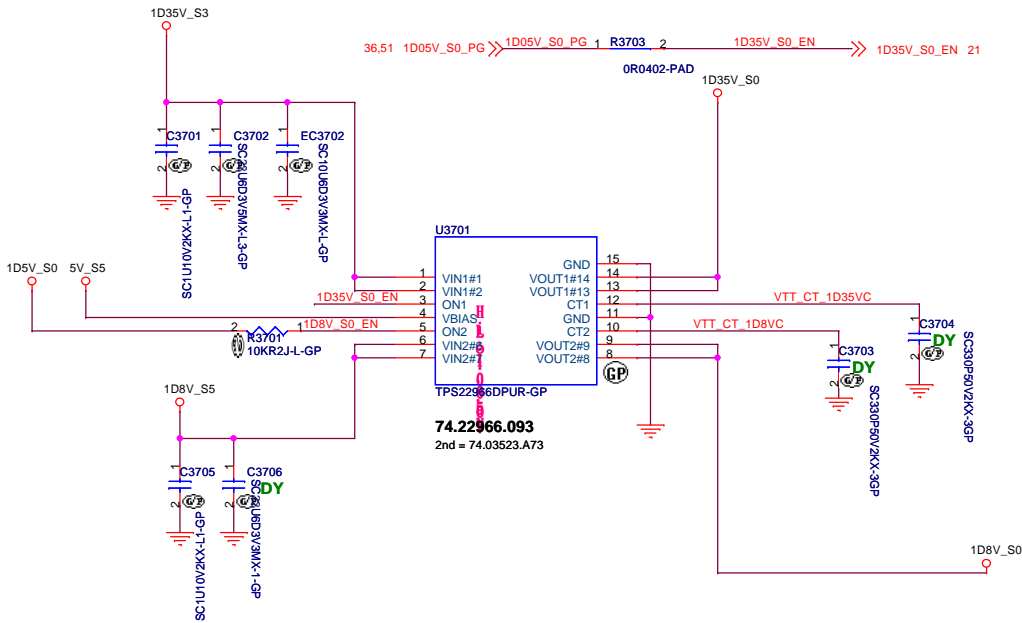
To EC

COREPWROK

ANNIE Run Power

Discharge circuit

1D35V_S0 1D8V_S0



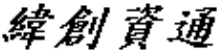
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Title			
ADAPTER OCP / S3 reduction			
Size A3	Document Number LF14B		Rev SA
Date: Thursday, April 10, 2014	Sheet 37	of 102	

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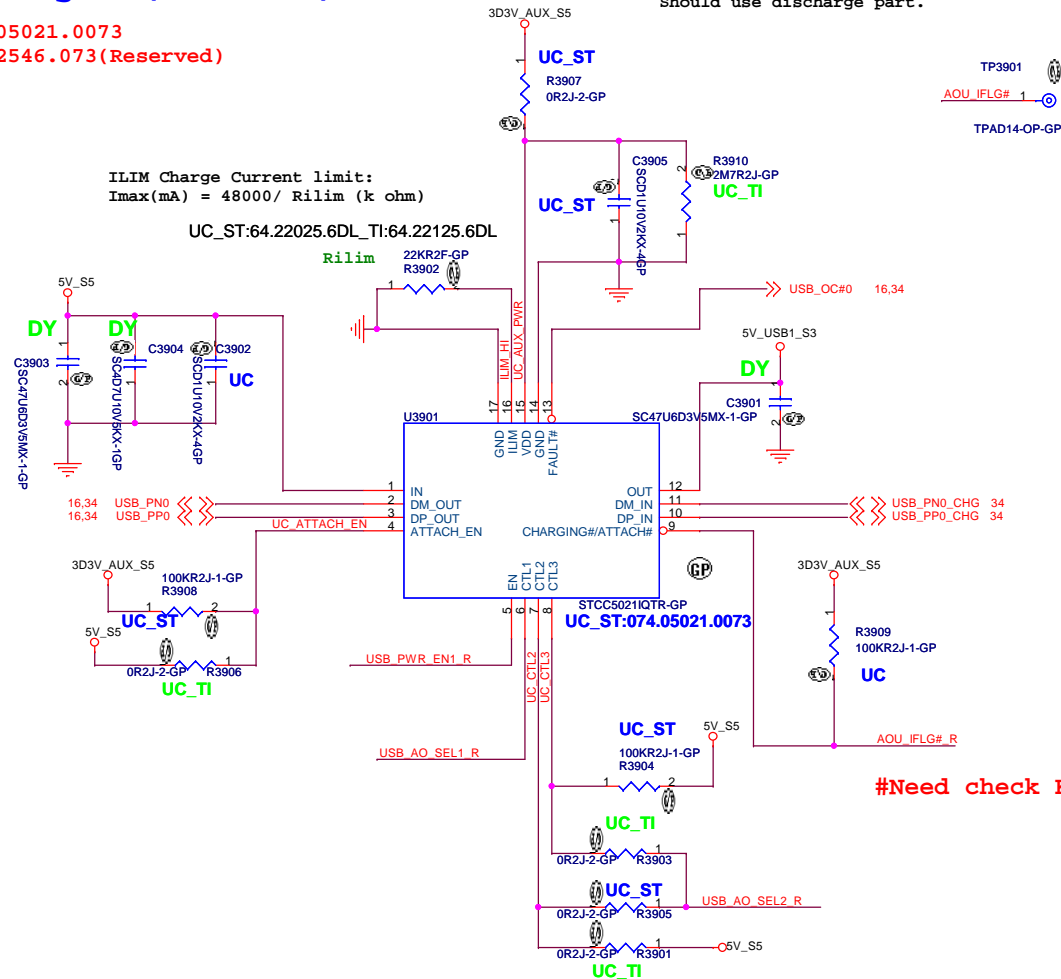
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Title (Reserved)			
Size A4	Document Number LF14B		Rev SC
Date: Tuesday, October 22, 2013		Sheet 38 of	102

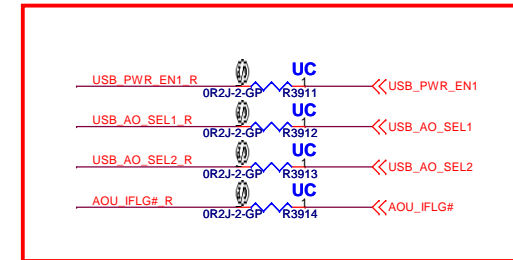
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# ST:074.05021.0073
TI:74.02546.073(Reserved)
```

2013/9/10 Change Power Source to 5V_S5
2013/9/18 Change Charger IC to STCC5021

Should use discharge part.



20131009
?????



#Need check KBC GPIO Port is PSL_IN

STCC5021 Truth Table

Table 5. Truth table control pins CTLx

Host state	CTL1	CTL2	CTL3	Mode description
S0, S1	1	1	1	CDP BC1.2 with charging detection.
S3	0	1	1	CDP with remote wakeup for low-speed USB devices / DCP auto-mode for full-speed or high-speed USB devices or after a USB device detached
S4, S5	0	0	1	DCP auto-detect mode without remote wakeup, with charging detection

Table 6. Attach detector truth table

ATTACH_EN	EN	Attach detector
0	x	OFF
1	1	OFF
1	0	ON

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Title

USB Charger

Size
A3

	Document Number
--	-----------------

Rev
SA


Date: Wednesday, April 16, 2014

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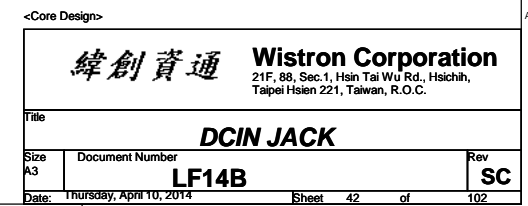
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Title Reserved			
Size A4	Document Number LF14B		Rev SA
Date: Thursday, February 13, 2014		Sheet 40 of	102

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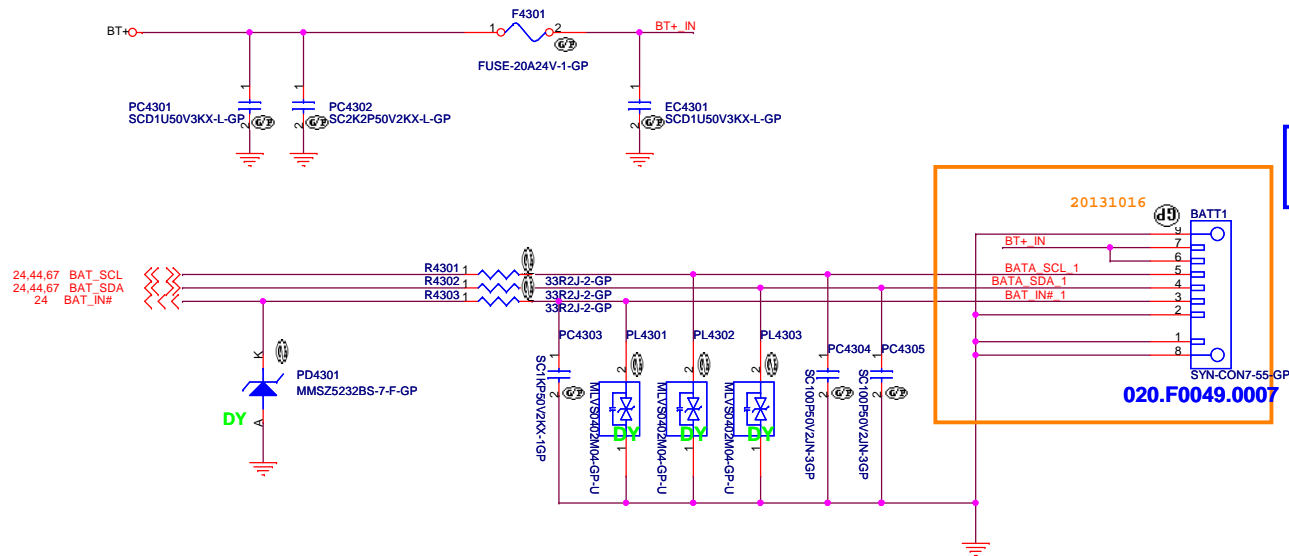
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Reserved			
Size	Document Number		Rev
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Adaptor in to generate DCBATOUT

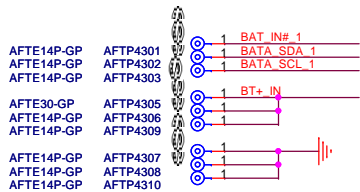


BATTERY CONNECTOR



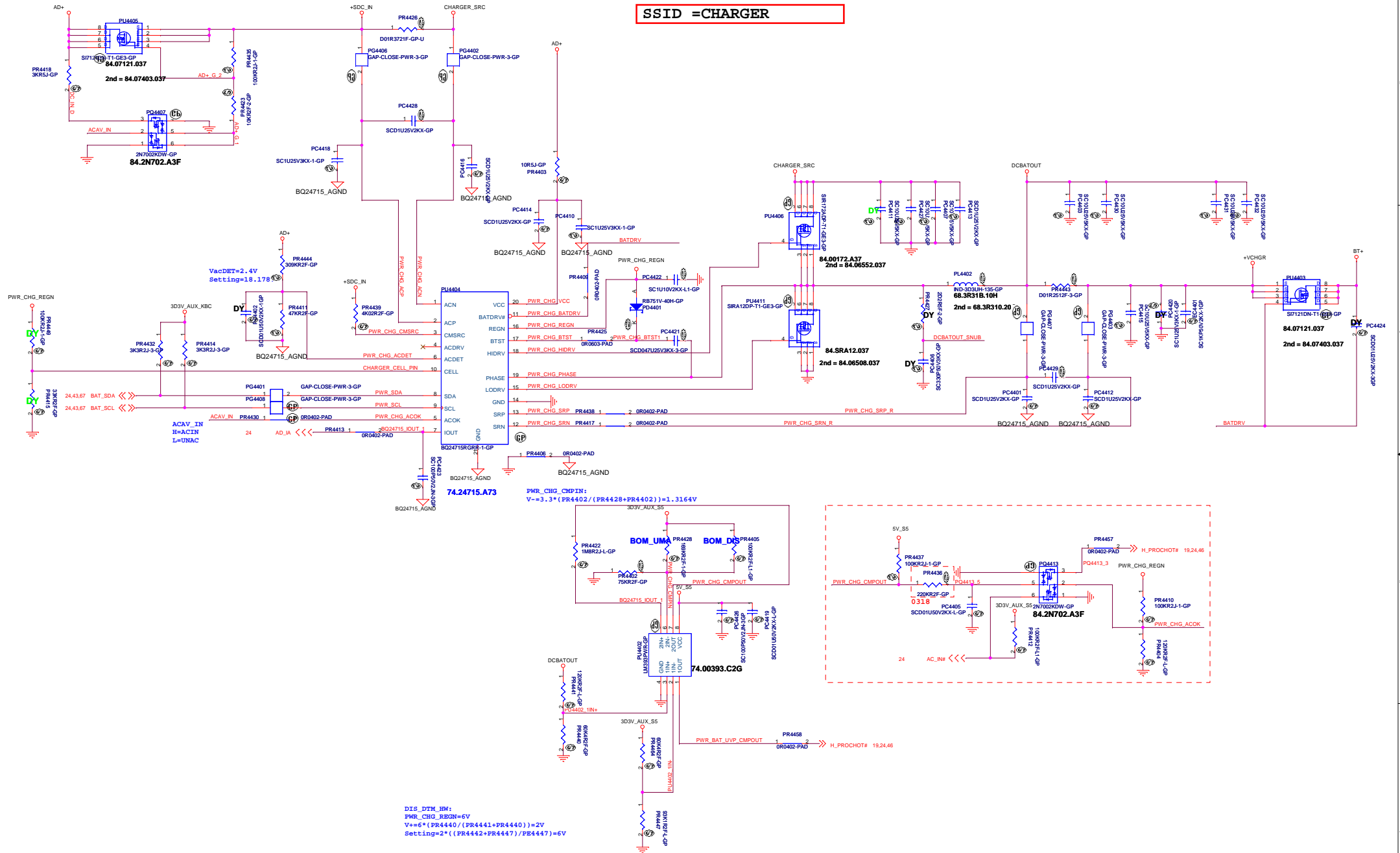
2013/10/4
Pin Define

Pin#	Comments	Color
1	GND-	BLACK
2	GND-	BLACK
3	ID	WHITE
4	SMD	GREEN
5	SMC	BLUE
6	BATT+	RED
7	BATT+	RED



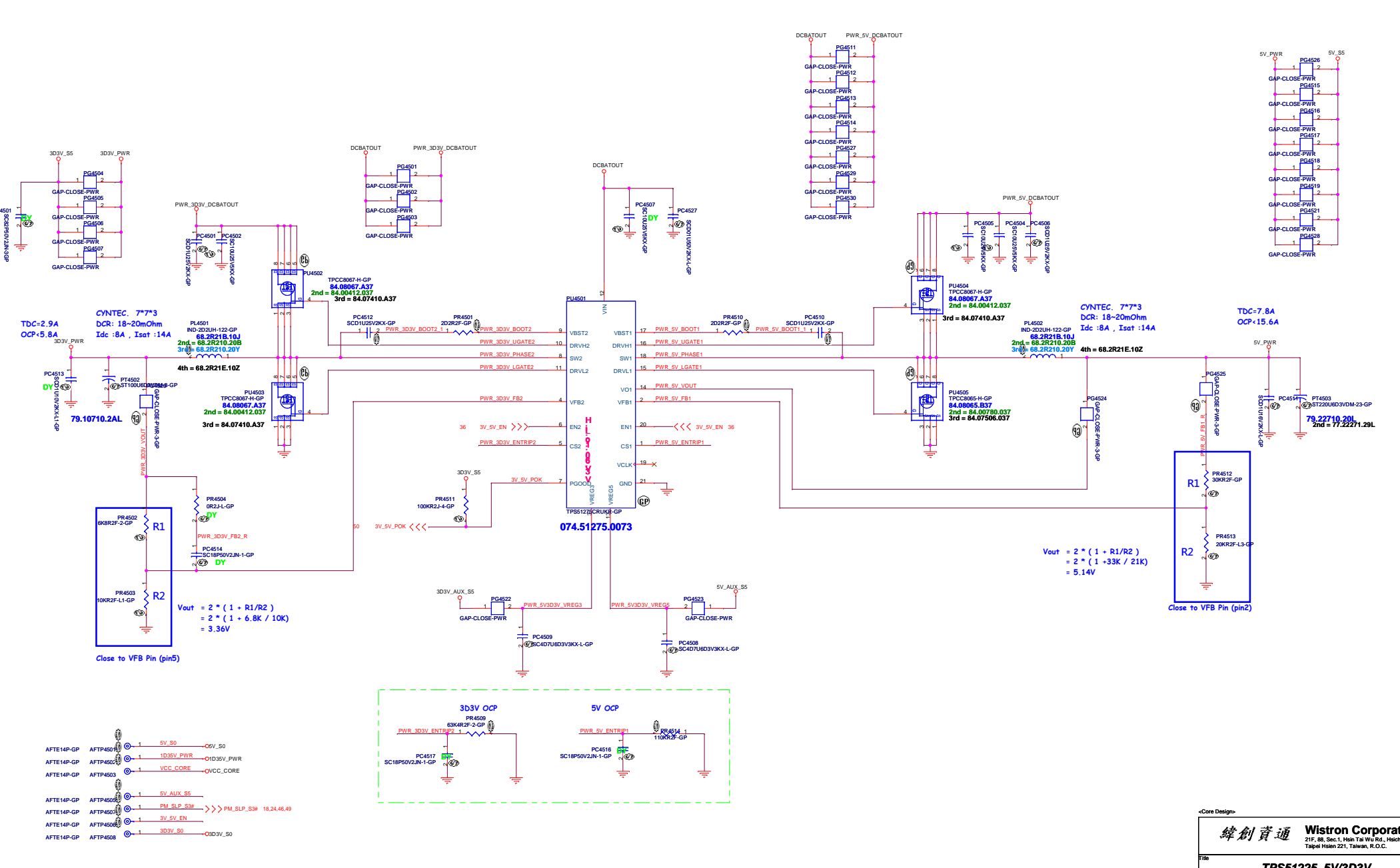
<Core Design>

SSID =CHARGER

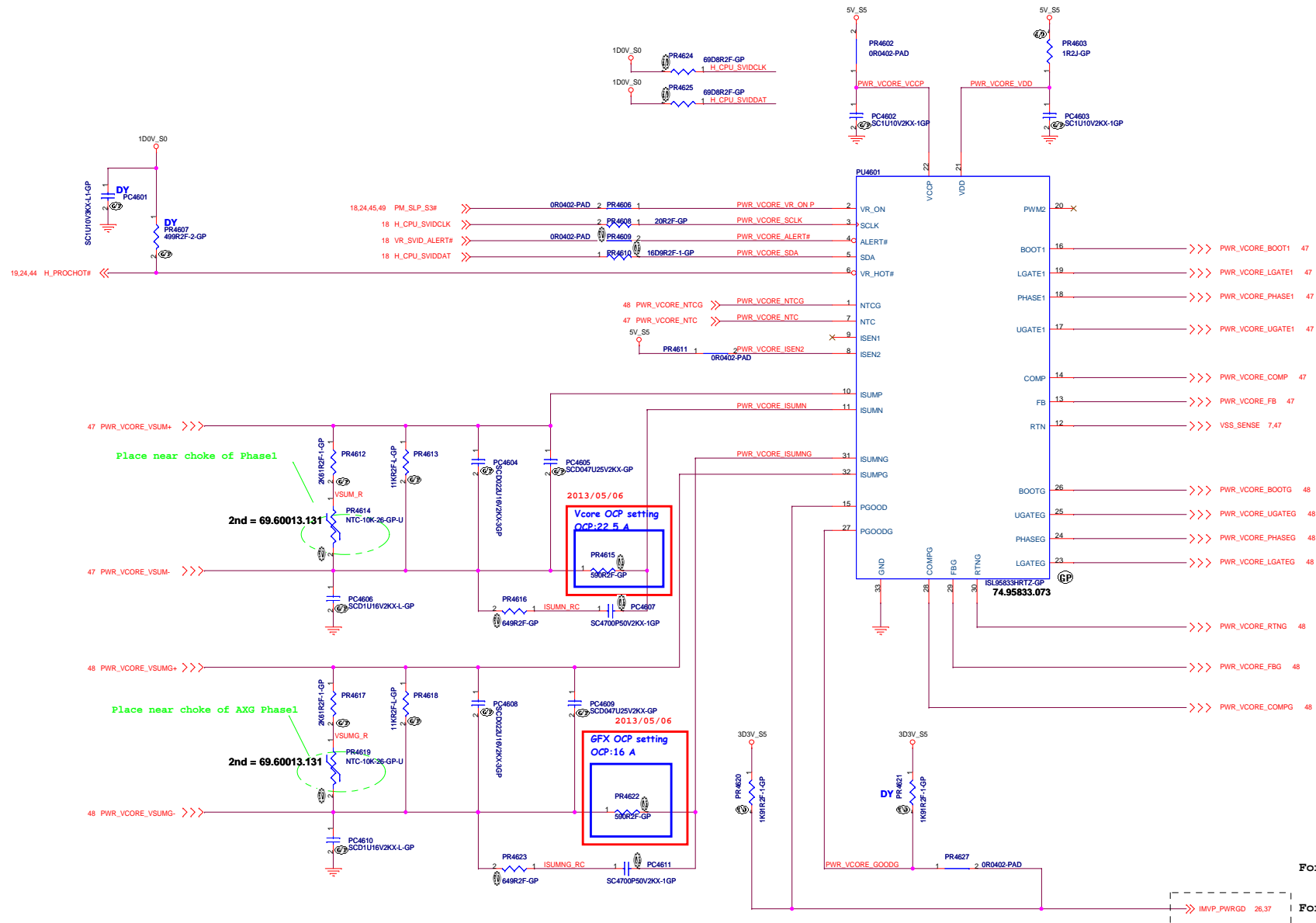


Core Design

```
SSID = PWR.Plane.Regulator_3p3v5v
```

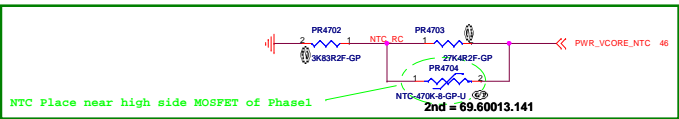
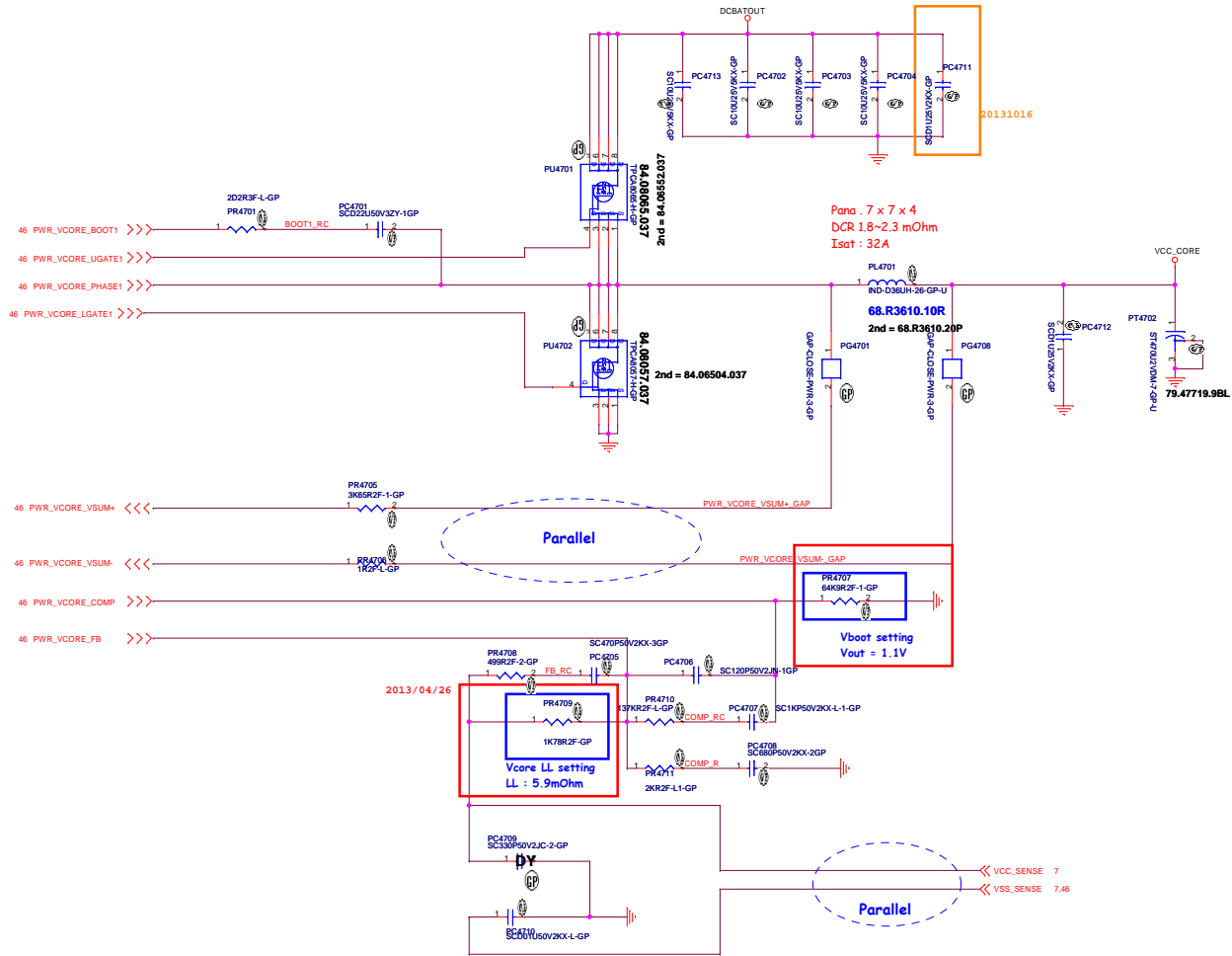


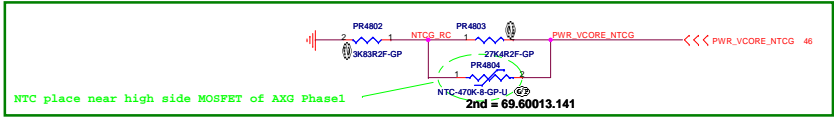
SSID = CPU.Regulator



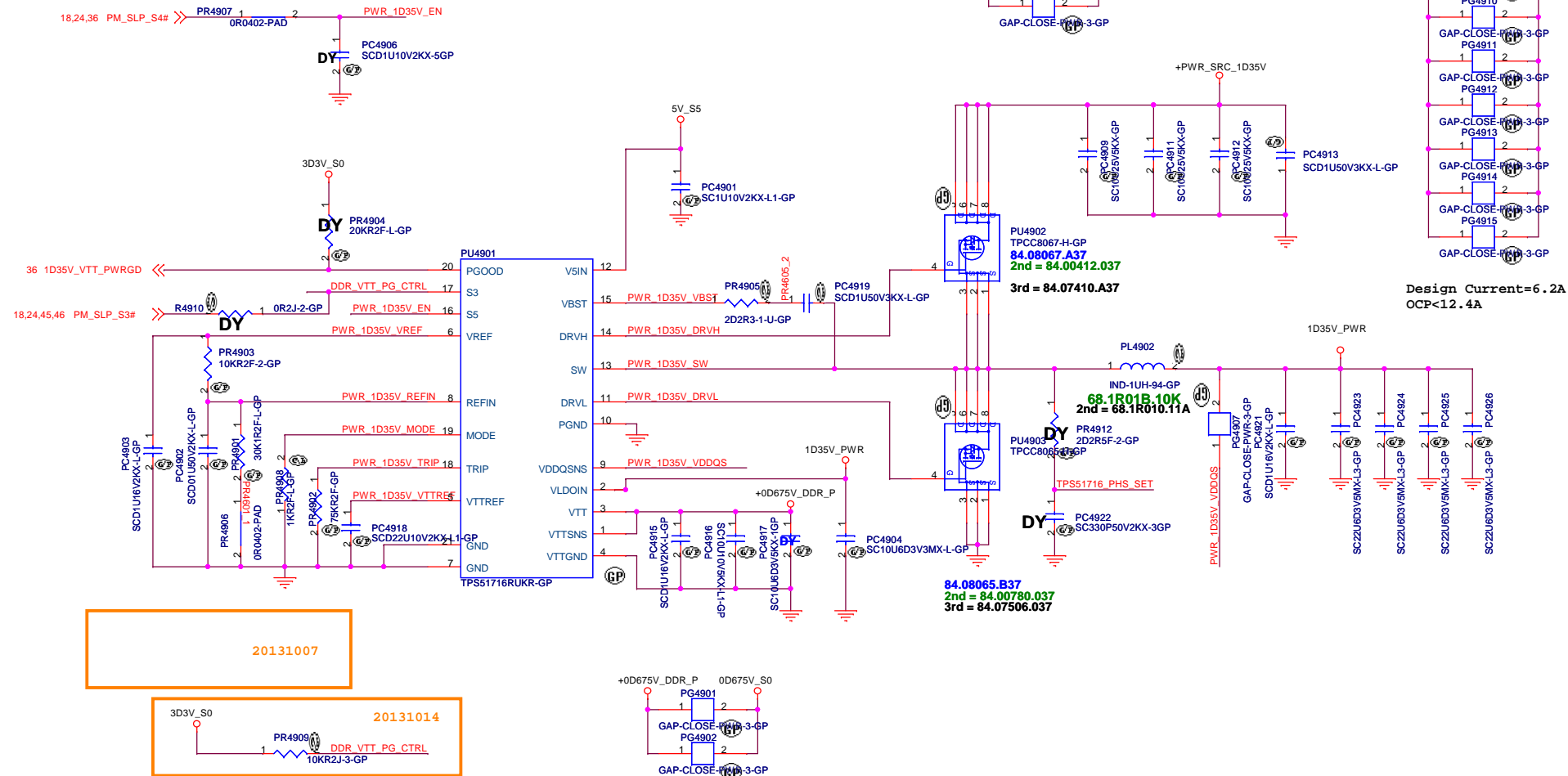
For GFX

```
| For VCCCORE
```





SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L

Inductor:CHIP CHOKE 0.68UH PCMC104T-R68MN 2.4~2.7mohm Isat =39Arms68.R6810.20G

O/P cap:CHIP CAP C 22U 6.3V M0805 X5R / 78.22610.51L

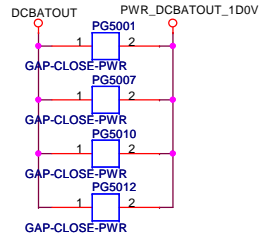
MOS: FET MOS FDMS3664S NC POWER56 / 84.03664.037 / Q1: 8.5~11mohm @Vgs=4.5V Q2: 2.6~3.2mohm @Vgs=4.5V

<Core Design>

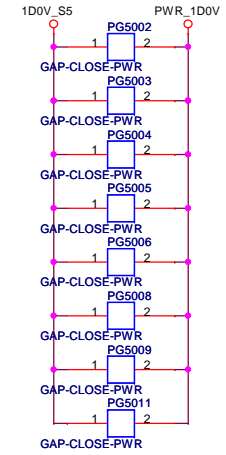
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Title			
TPS51716 1D35V & 0D675V			
Size A3	Document Number		Rev
			X00
Date:	Thursday, April 10, 2014	Sheet 49 of	102

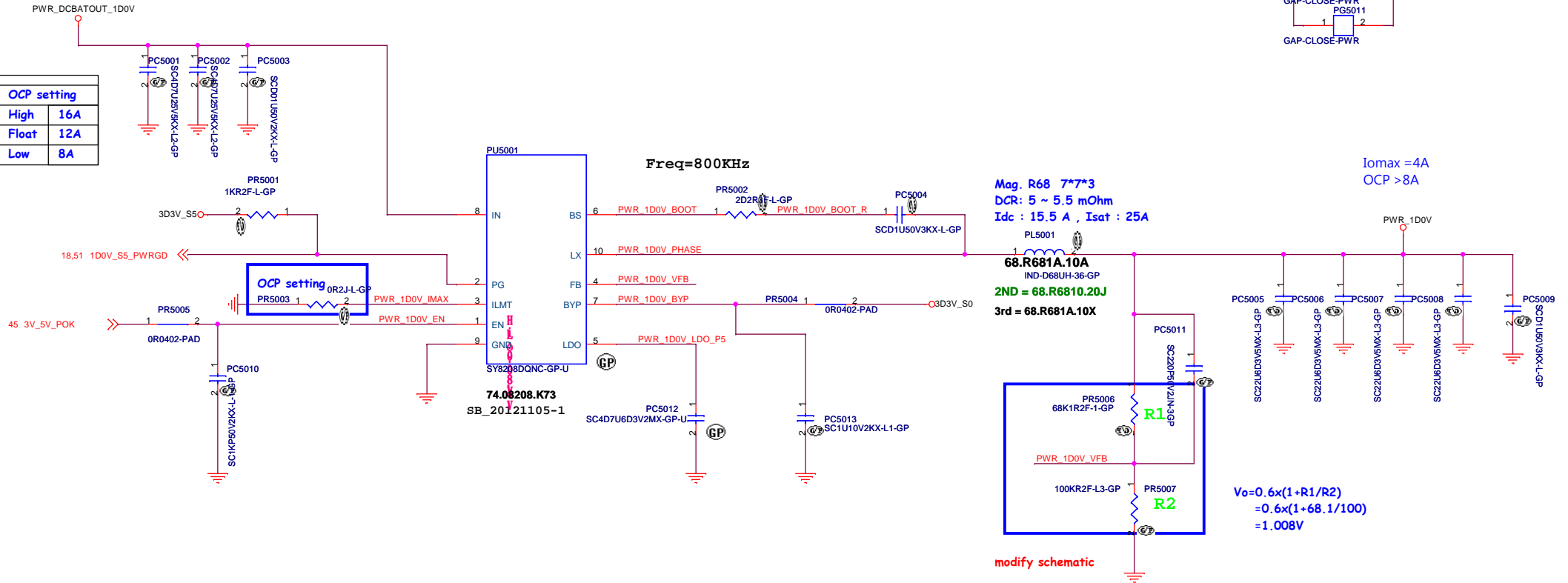
SB_20121105-1



SY8208D for 1D0V_S5
Enable=0.8V
Disable=0.4V



OCP setting	
High	16A
Float	12A
Low	8A

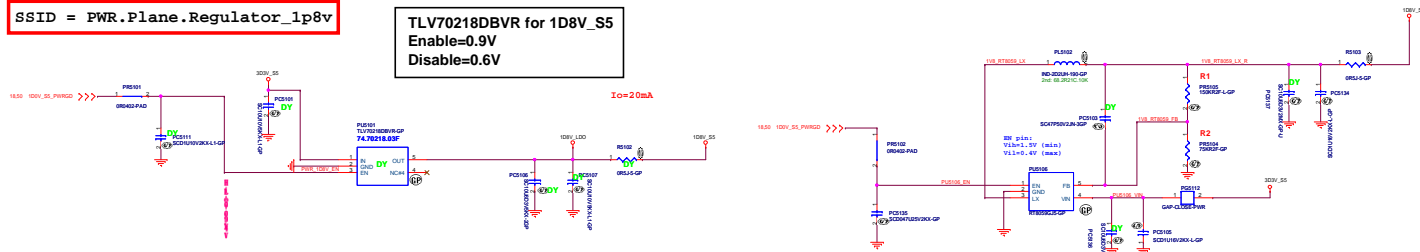


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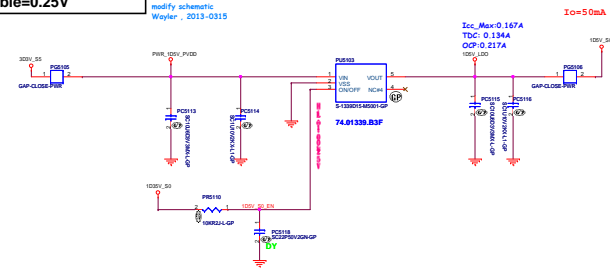
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<p>Title: DC to DC 1D05V(SY8208D)</p>	
Size A3	Document Number LF14B
Date: Thursday, April 10, 2014	Rev SA
<p>Sheet 50 of 102</p>	

TLV70218DBVR for 1D8V_S5 Enable=0.9V Disable=0.6V
--

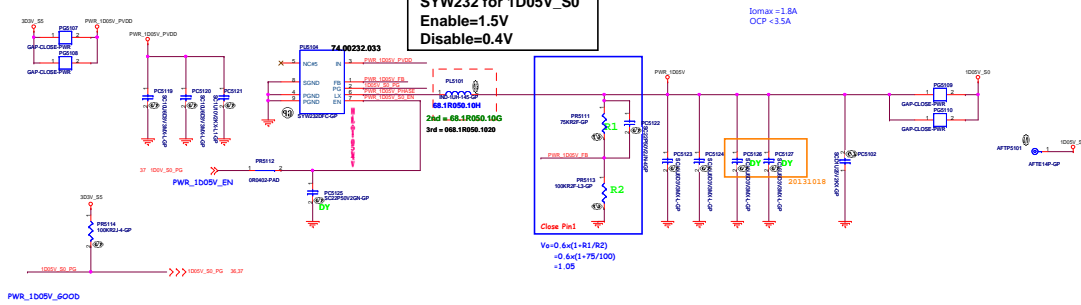


modify schematic
Wayler , 2013-0315

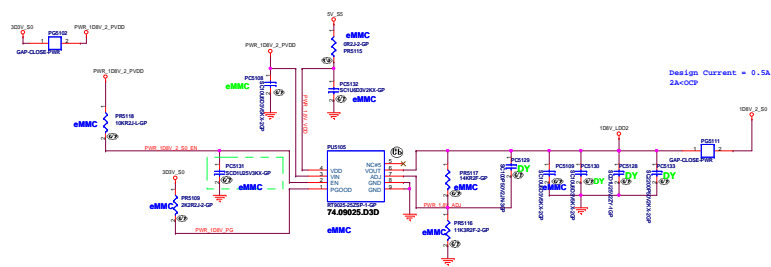


SYW232 for 1D05V_S0
Enable=1.5V
Disable=0.4V

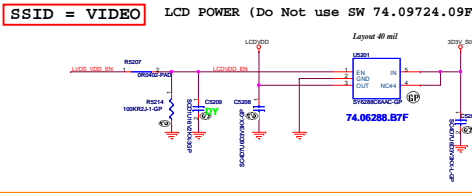
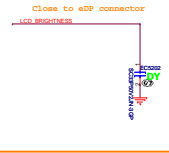
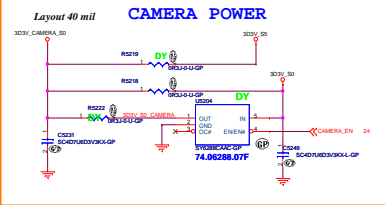
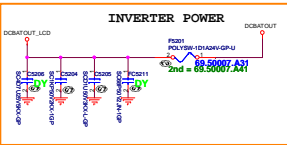
I_{max} = 1.8A
OCP < 3.5A



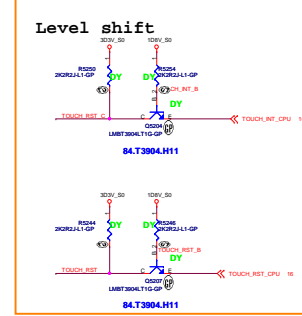
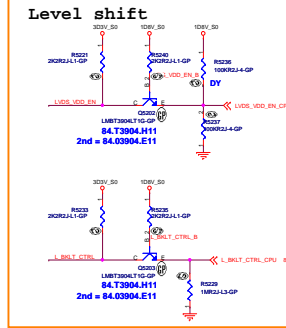
RT9025 for 1D8V_S5



SSTD = VIDEO



Panel BL brightness/Power En/BL Er

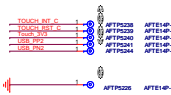
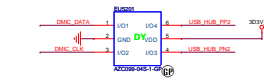
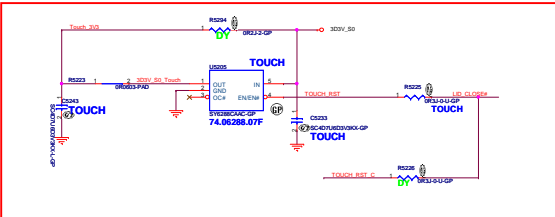
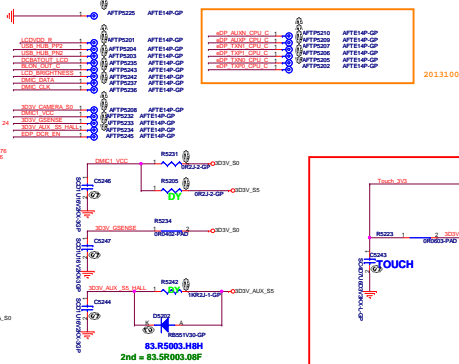
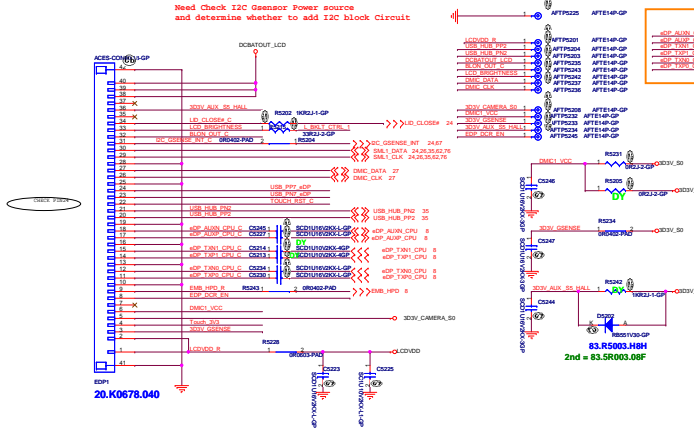


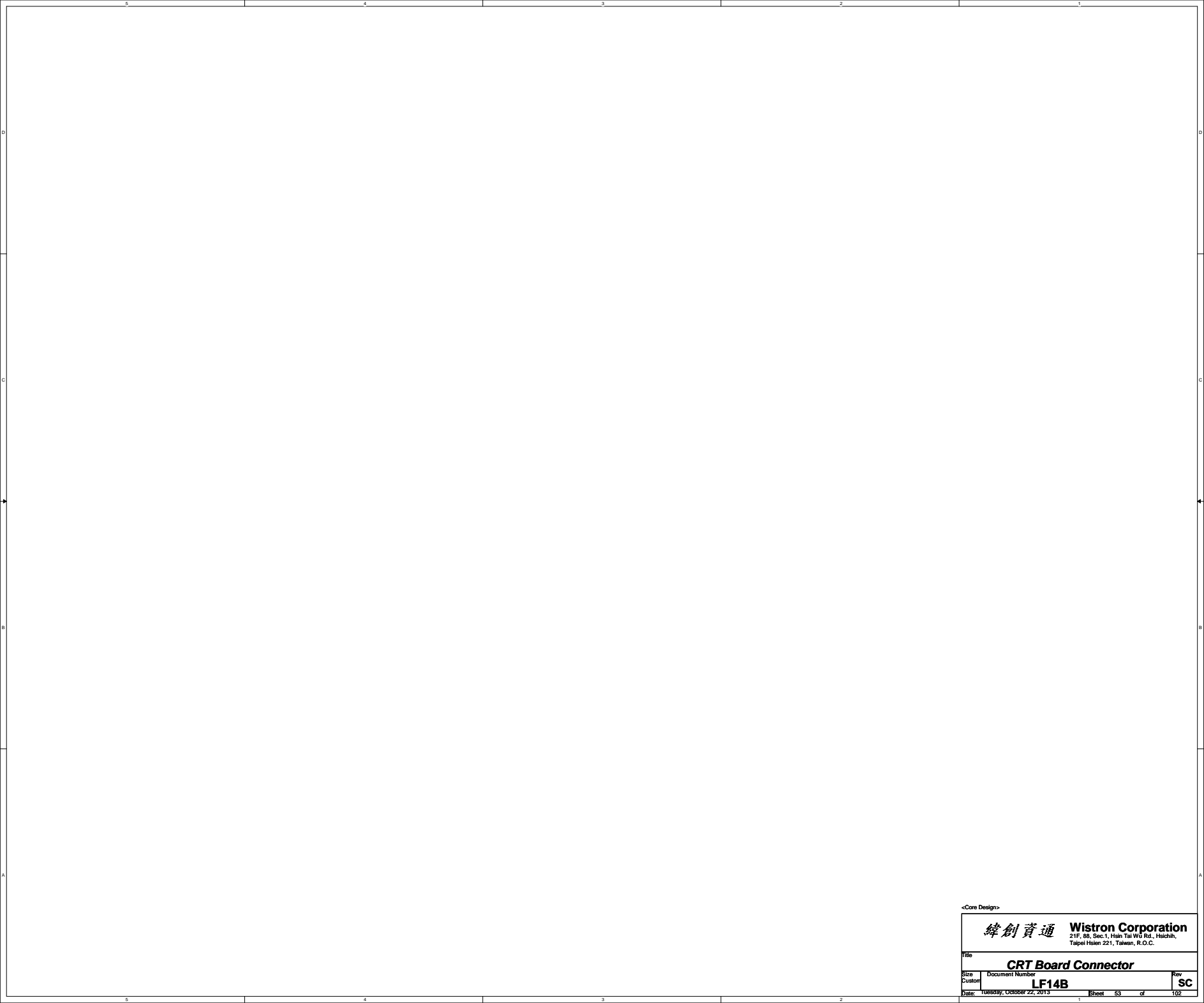
eDP connector

2-lane eDP Compare with LM440T 12306-1

BLON_OUT_C:LM440T PCH->EC->PANE

eDP HPD:LM440T & LE443 invert to eDP HPD



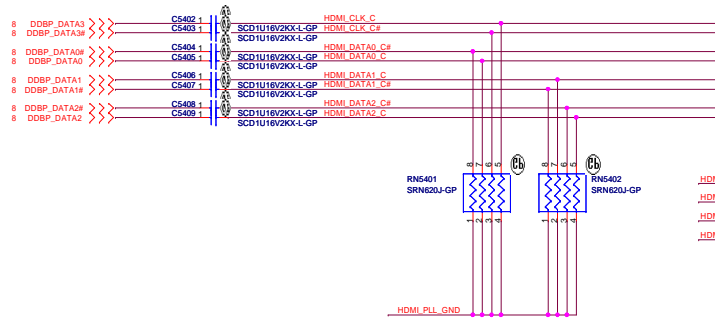


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<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
CRT Board Connector		
Size	Document Number	Rev
Custom	LF14B	SC
Date: Tuesday, October 22, 2013		
Sheet 53 of 102		

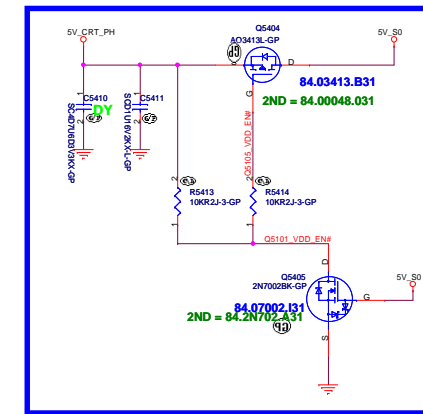
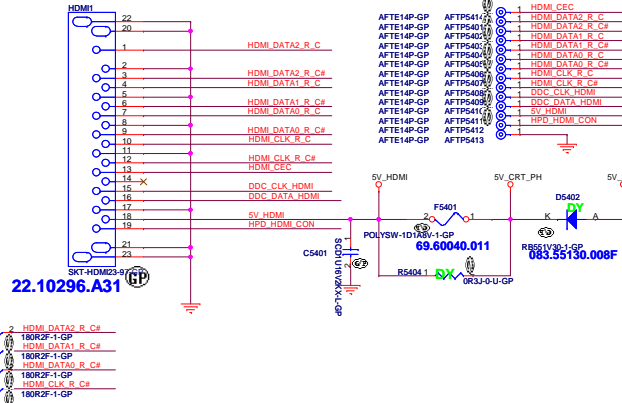
SSID = VIDEO

HDMI Passive Level Shifter

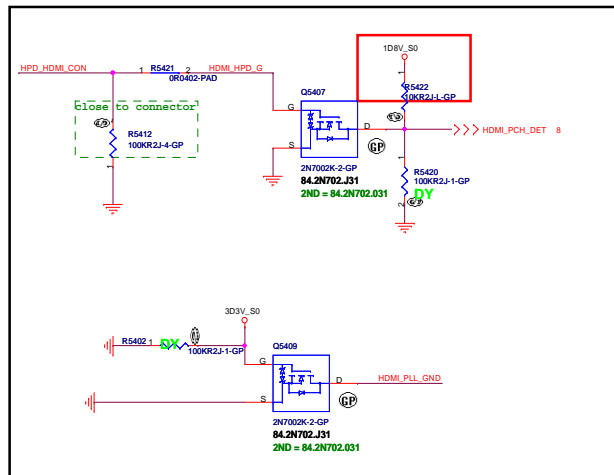
Close to HDMI Connector



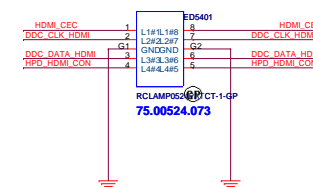
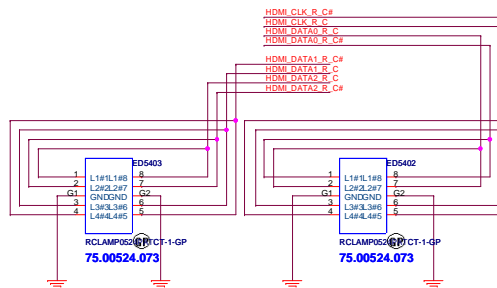
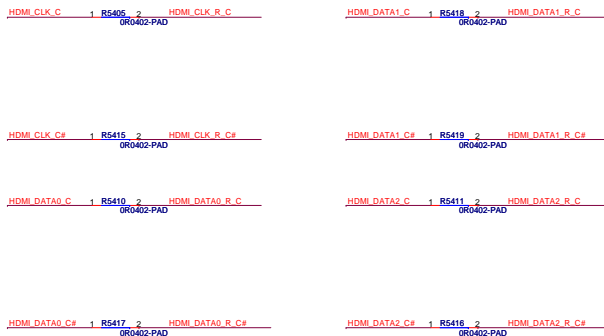
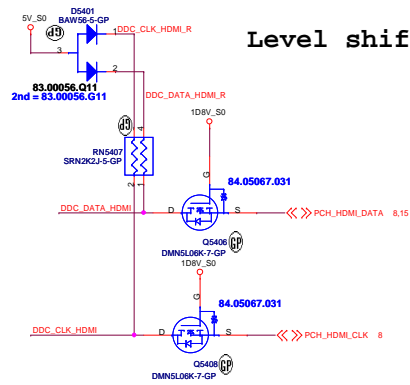
HDMI CONNECTOR



HDMI DDC Passive Level Shifter



Level shift



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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

TRAVIS

Size
A2

Document Number
LF14B

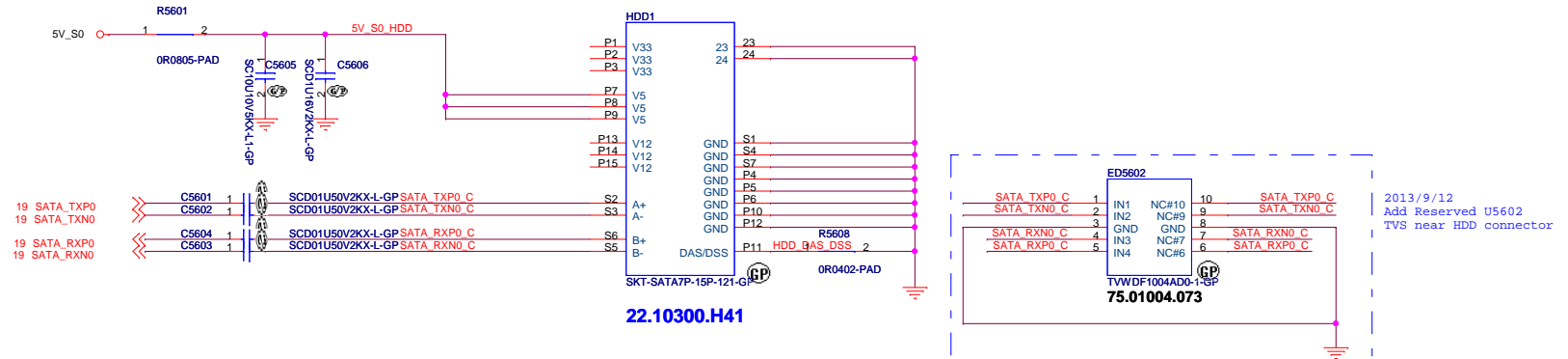
Rev
SC

Date: Tuesday, October 22, 2013

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SSID = SATA

SATA HDD Connector



ODD Connector

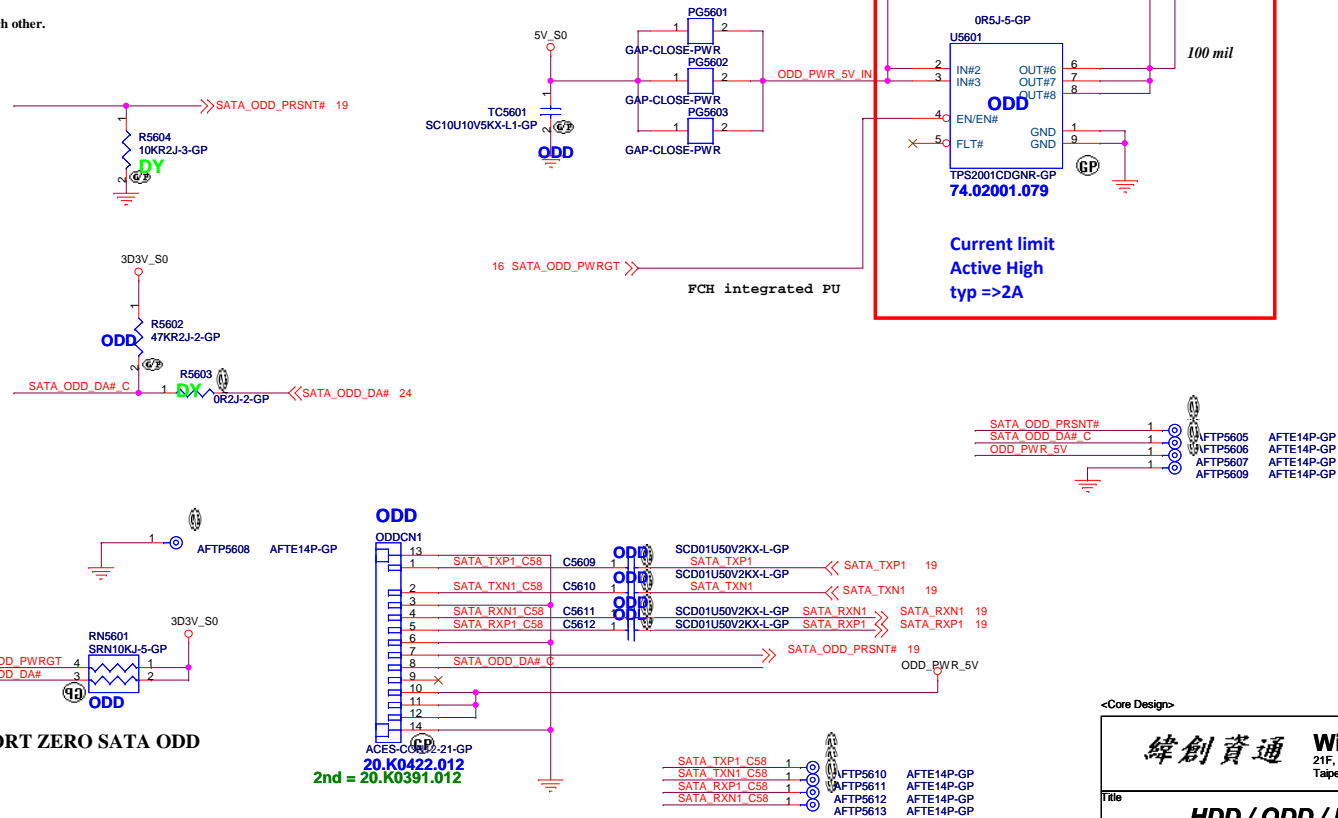
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil
Mars:
Exchange ODD and ESATA differential pair each other.

Follow Intel Zero Power ODD SPEC

ODD (M50/U50)

Need Check 2spindle series & Components

~~SATA Zero Power ODD~~



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Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD / ODD / NGFF_SSD

Size	
------	--

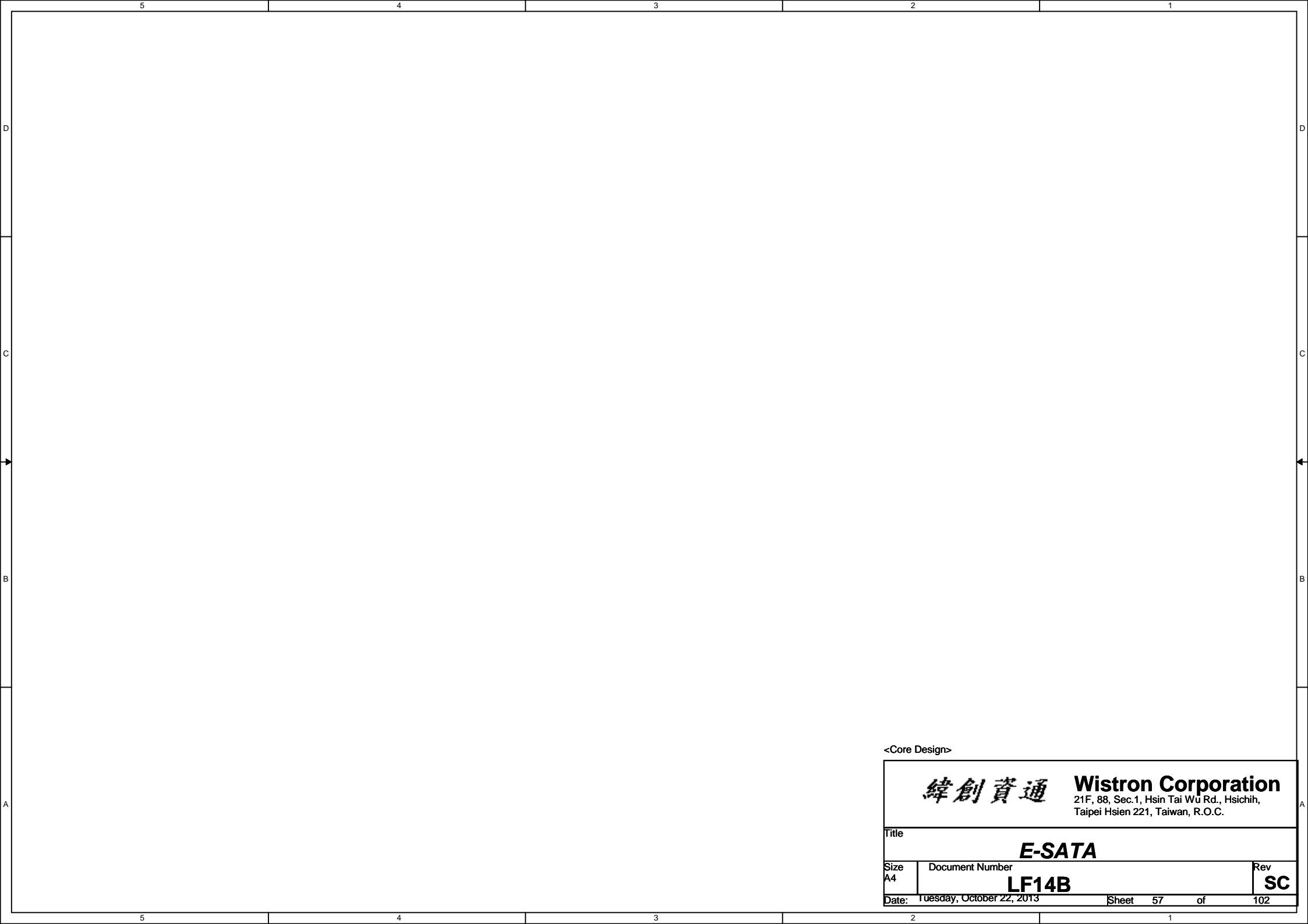
Document Number

Number

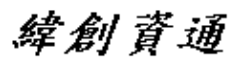
Rev

Customer: **LF1**
Date: Wednesday, April 16, 2014

			SC
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
E-SATA			
Size A4	Document Number LF14B		Rev SC
Date:	Tuesday, October 22, 2013		Sheet 57 of 102



SSID = Wireless

Mini Card Connector(mSATA)

<Core Design>

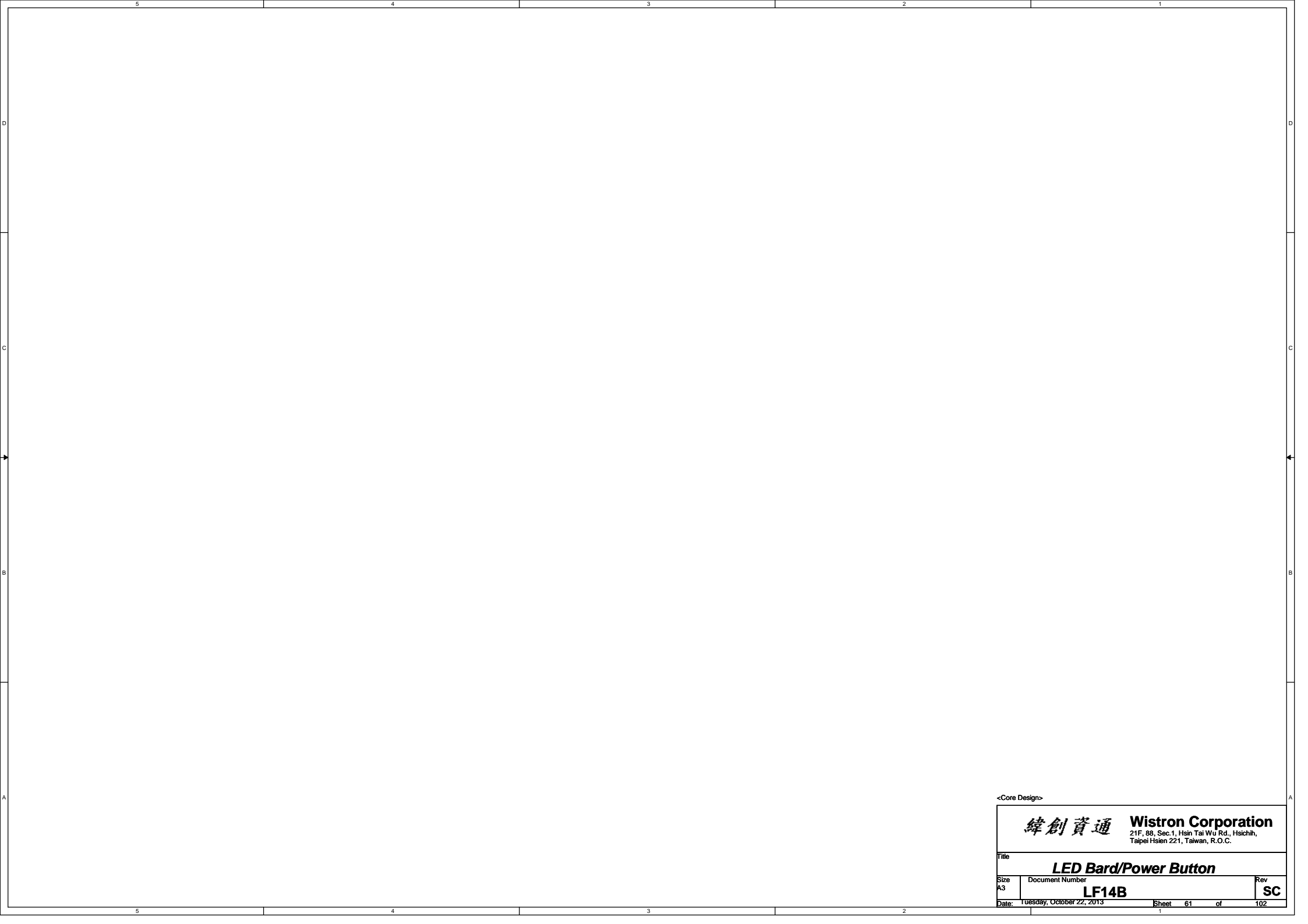
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Title <div>WWAN CONN</div>		
Size <div>A4</div>	Document Number <div>LF14B</div>	Rev <div>SC</div>
Date: Tuesday, October 22, 2013		Sheet 59 of 102

SSID = mSATA

Mini Card Connector(mSATA)

<Core Design>

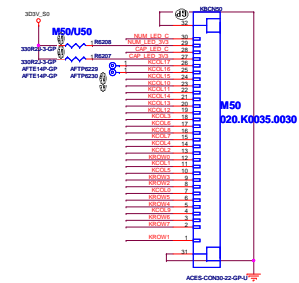
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
mSATA Connector			
Size	Document Number		Rev
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Date:	Tuesday, October 22, 2013		Sheet 60 of 102



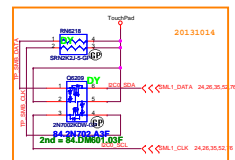
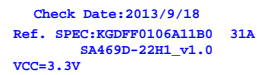
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LED Bard/Power Button			
Size	Document Number		Rev
A3	LF14B		SC
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Internal KeyBoard Connector

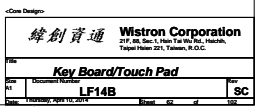


20131007



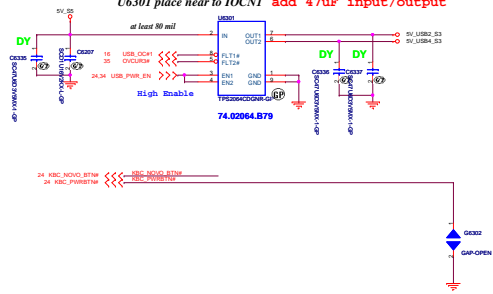
AFTE14P-GP AFTP6227 KB BL LED+
AFTE14P-GP AFTP6228 KB BL LED-

24 NUM_LED >>> G U6002 M50/U50
D NUM_LED_C
S
2N7002K-2-GP
84.2N702J31
2nd = 84.2N702.W31

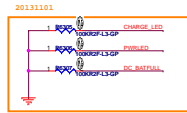


USB 2.0 port2/4 Power SW

U6301 place near to IOCN1 add 47uF input/output



IO BD M40/U40/M50/U50



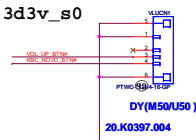
USB2.0 Card Reader

USB2.0 PORT
USB2.0 PORT



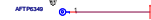
Volume BD M50/U50

+ PH 3d3v_s0

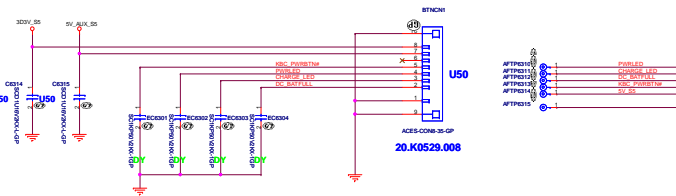


Need Check Pin Define

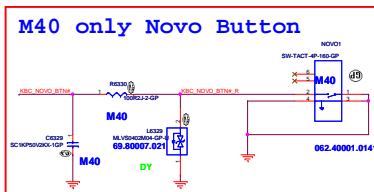
主板Pin定義不動
只動小板
小板Pin只接所需Pin
其餘GND

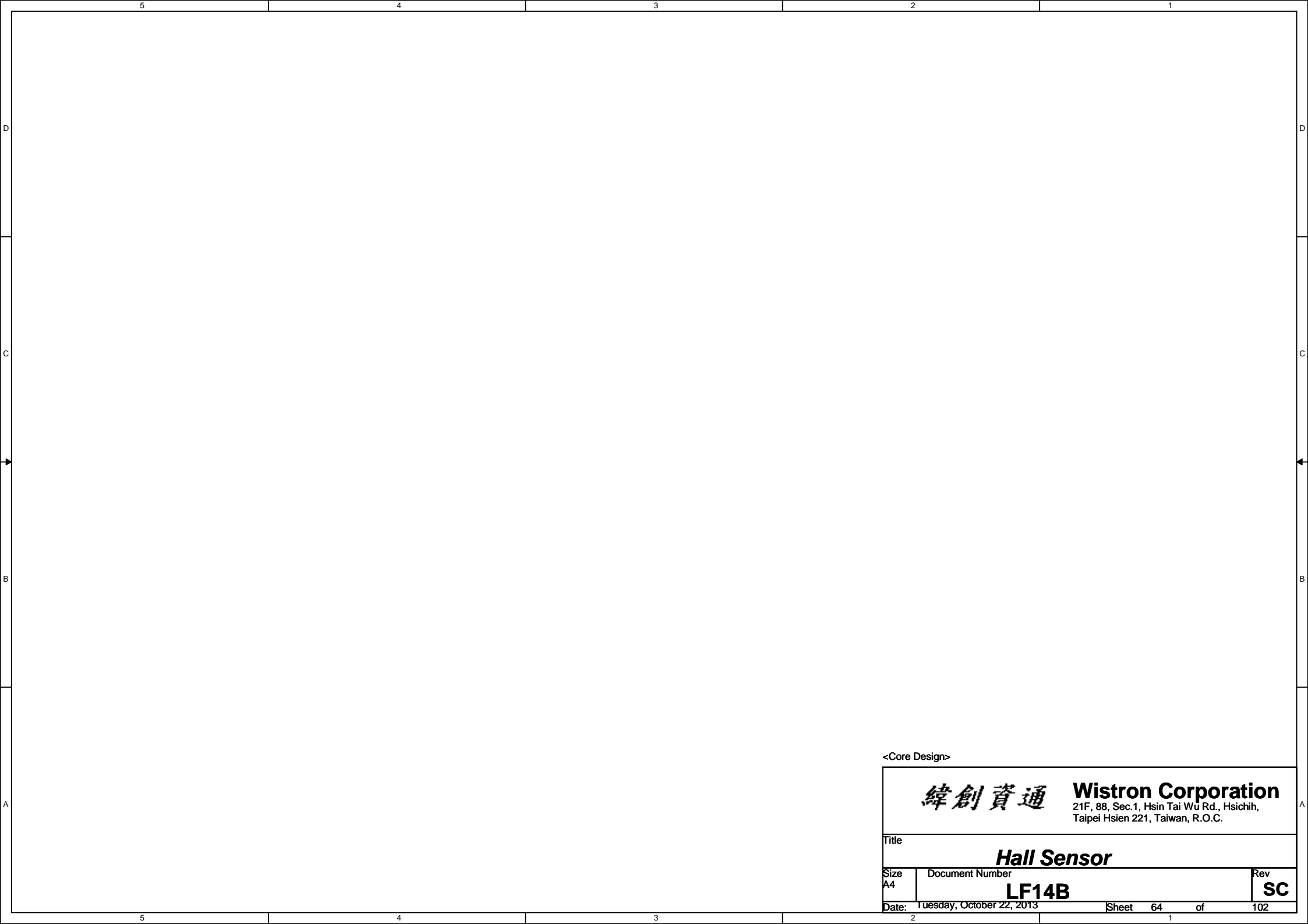


BTN BD U50 only



Novo Button M40 only





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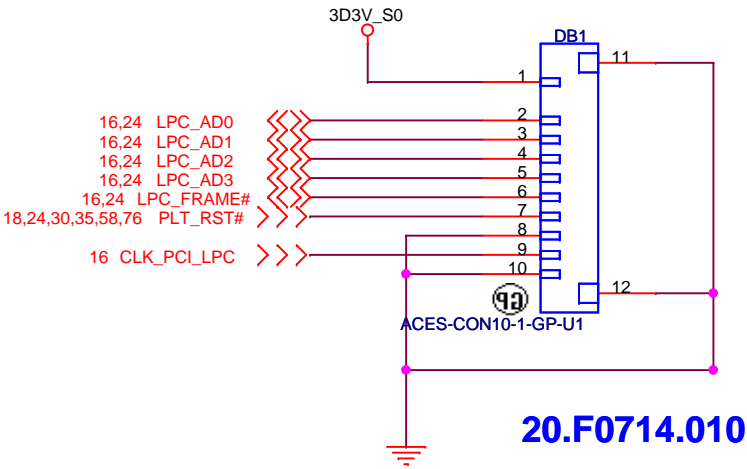
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

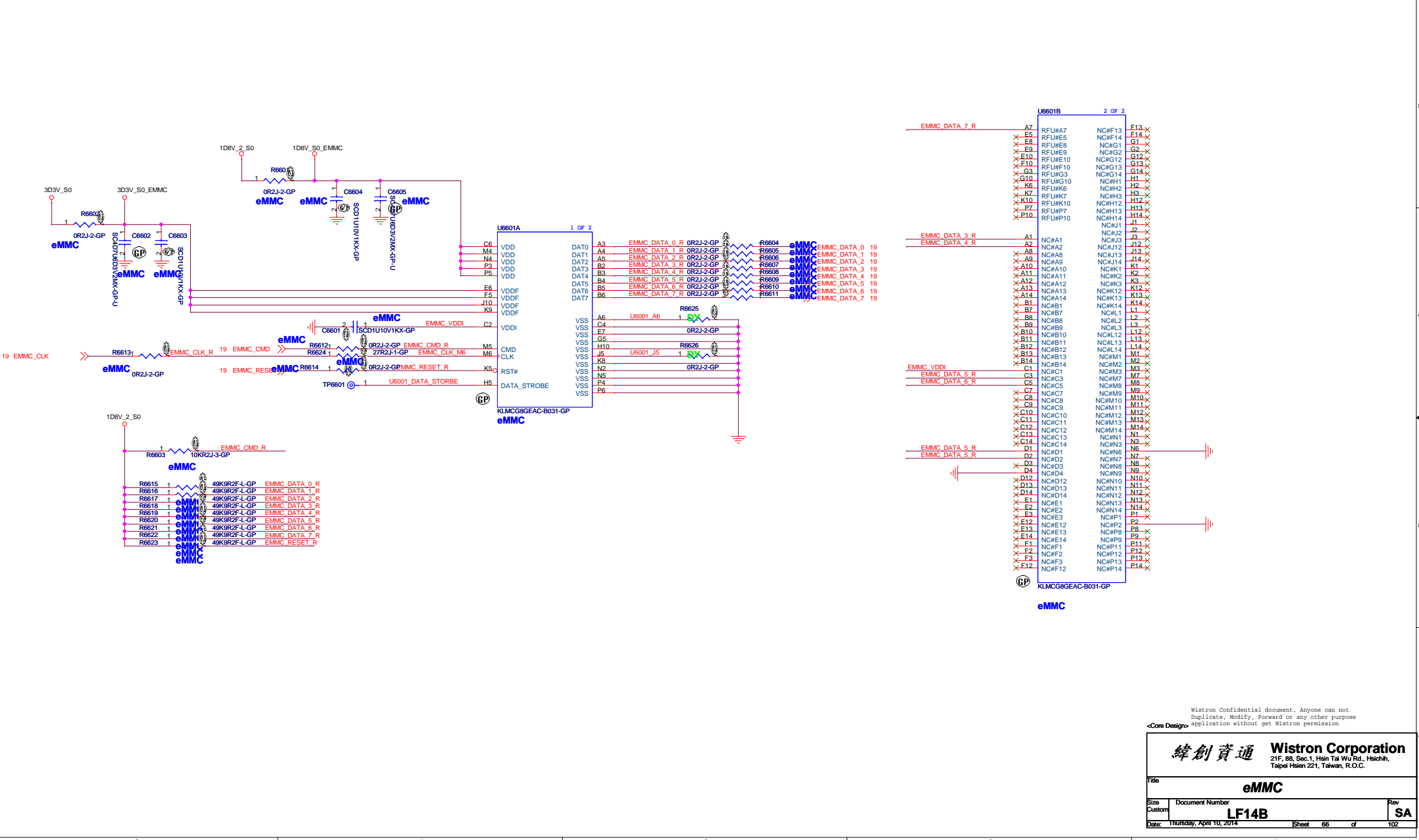
Size A4	Document Number LF14B	Rev SC
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Debug Connector



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Title			
<i>Dubug connector</i>			
Size A4	Document Number LF14B		Rev SC
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Title		
eMMC		
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Need Stuff

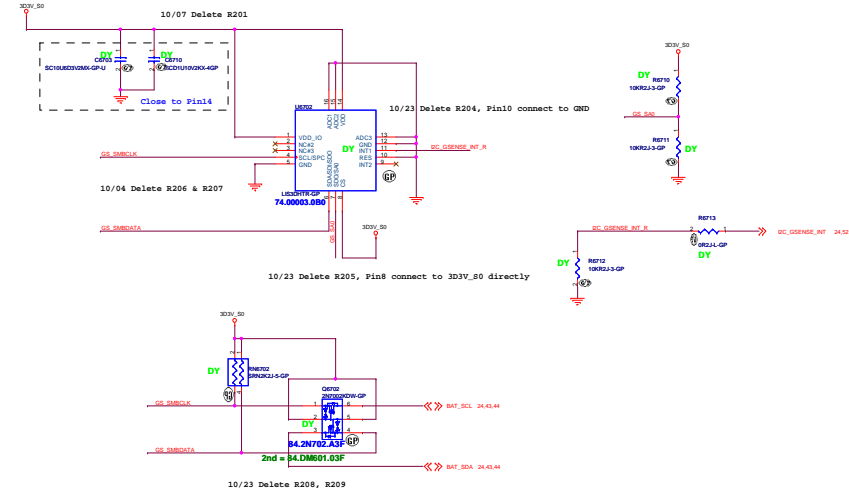


```
*CS="H"; mode="I2C"  
CS="L"; mode="SPI"
```

STMicro LIS34AL: 74.00034.0BZ
2nd = 74.KXTC8.0BZ

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



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Title

Thunderbolt (1/5)

Size
A4

Document Number

LF14B

Rev
SA

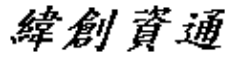
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Title Thunderbolt (2/5)			
Size A4	Document Number LF14B		Rev SA
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Title

Thunderbolt (3/5)

Size Custom

Document Number LF14B

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Title

Thunderbolt (4/5)

Size

A4

Document Number

LF14B

Rev

SA

Date: Thursday, February 13, 2014

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Title

Thunderbolt (5/5)

Size
A4

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Title

GPU(PEG)

Size
A2

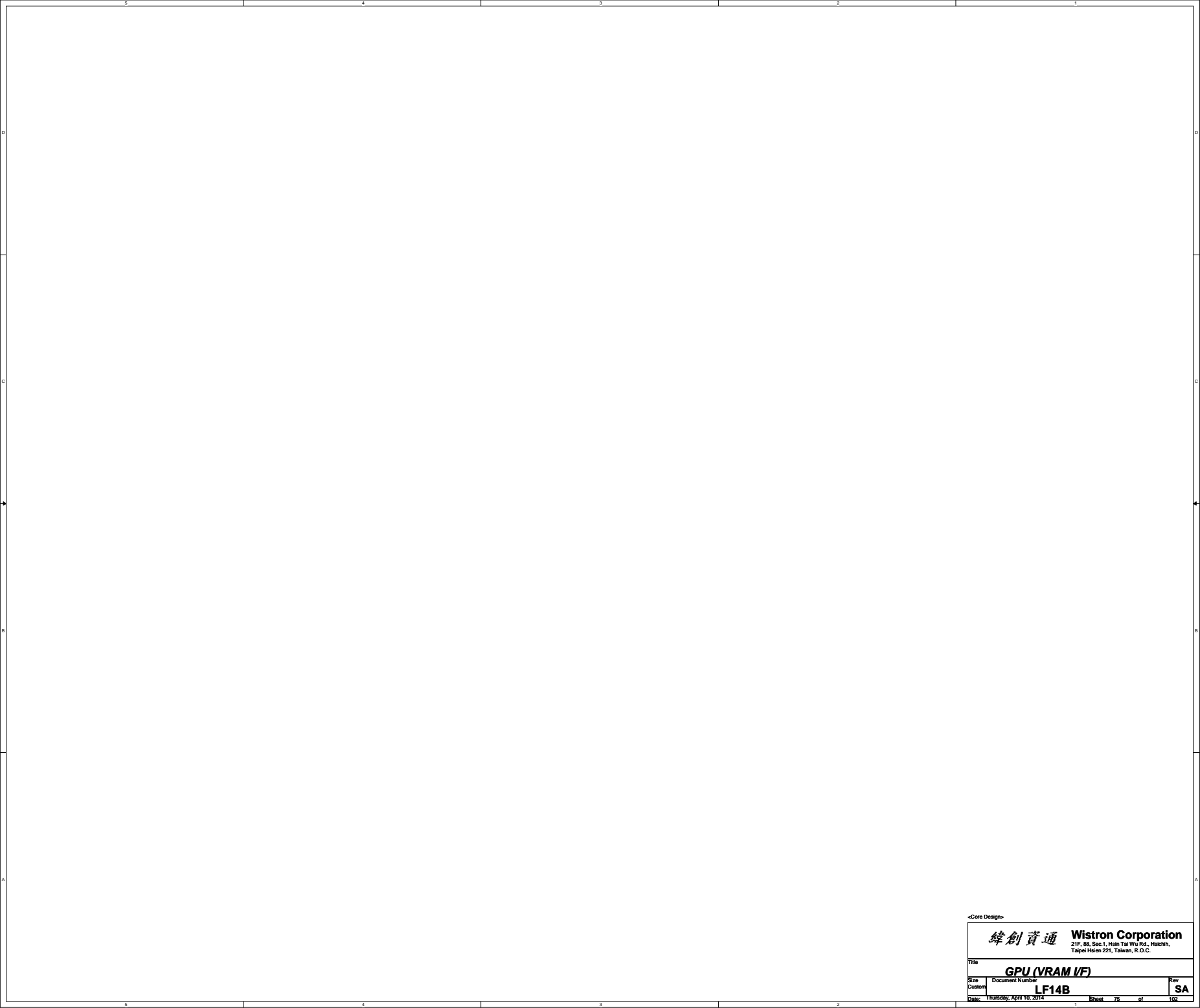
Document Number
LF14B

Date
Thursday, April 10, 2014

Rev.
SA

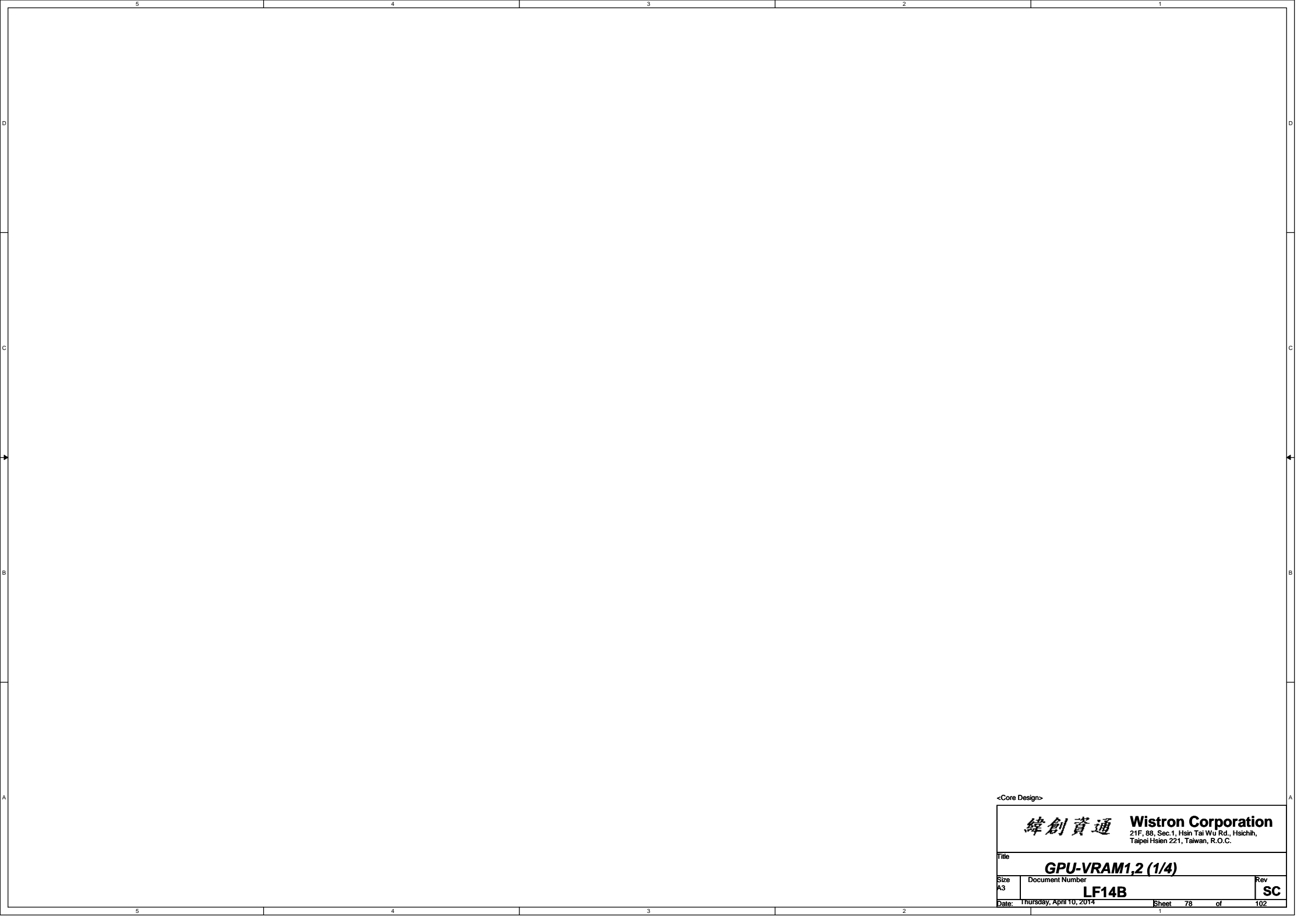
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<Core Design>		
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec-1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
GPU (VRAM I/F)		
Size	Document Number	Rev
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Title			
GPU-VRAM1,2 (1/4)			
Size	Document Number		Rev
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	5	4	3	2	1
D					
C					
B					
A					

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM3,4 (2/4)			
Size	Document Number		Rev
A3	LF14B		SC
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D				
C				
B				
A				

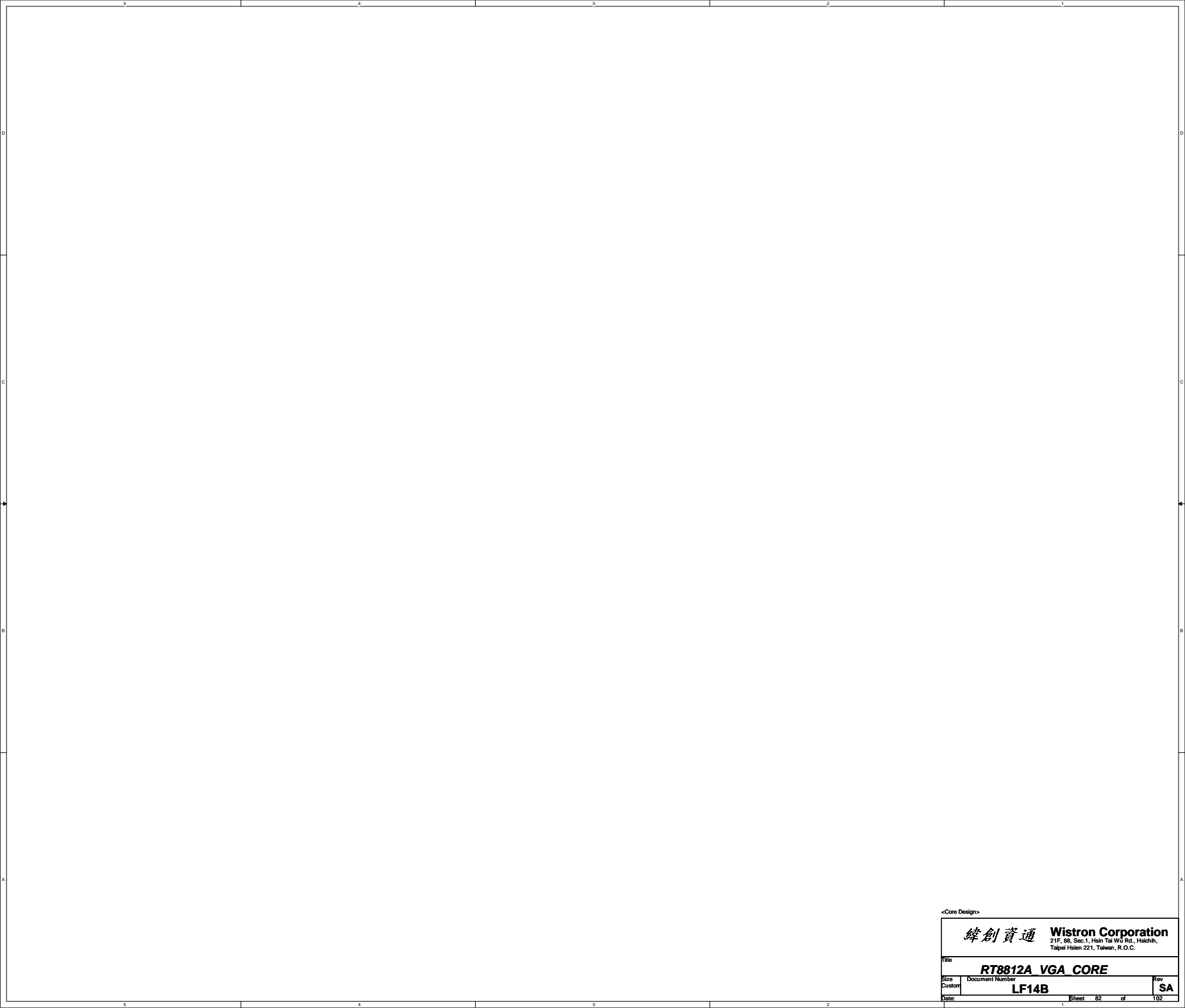
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM5,6 (3/4)			
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D				
C				
B				
A				

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Title			
GPU-VRAM7,8 (4/4)			
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File

RT8812A VGA CORE

Size
Custom

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LF14B

Rev
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Date

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Switchable GFX LCD(1/2)

Size
A4

Document Number

LF14B

Rev
SA

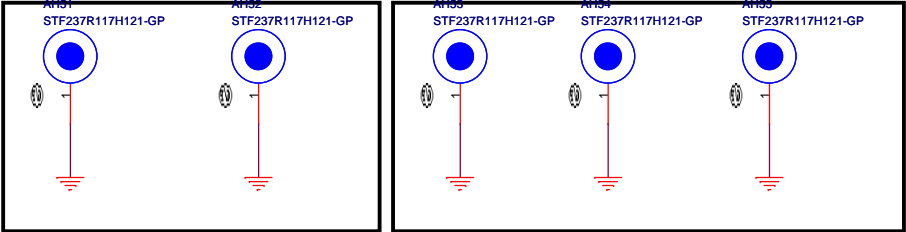
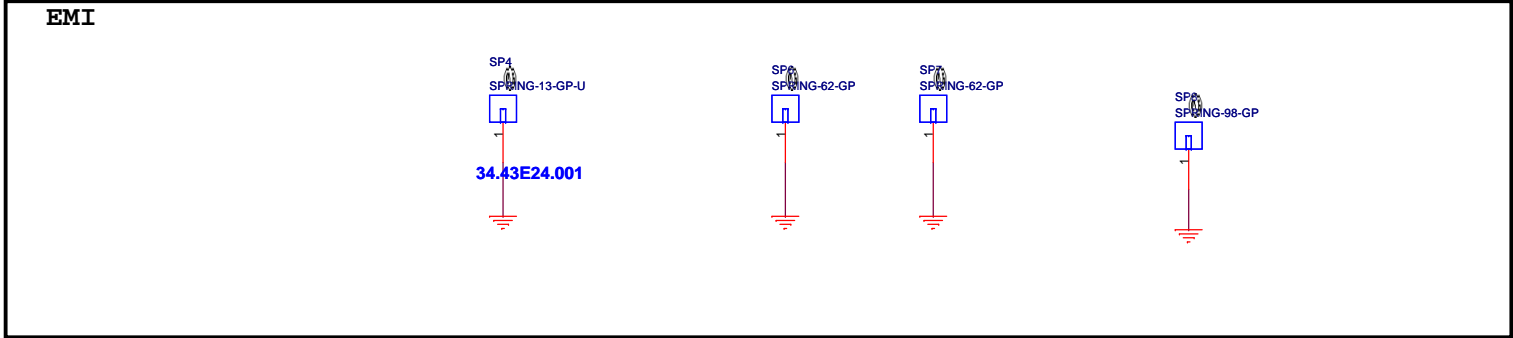
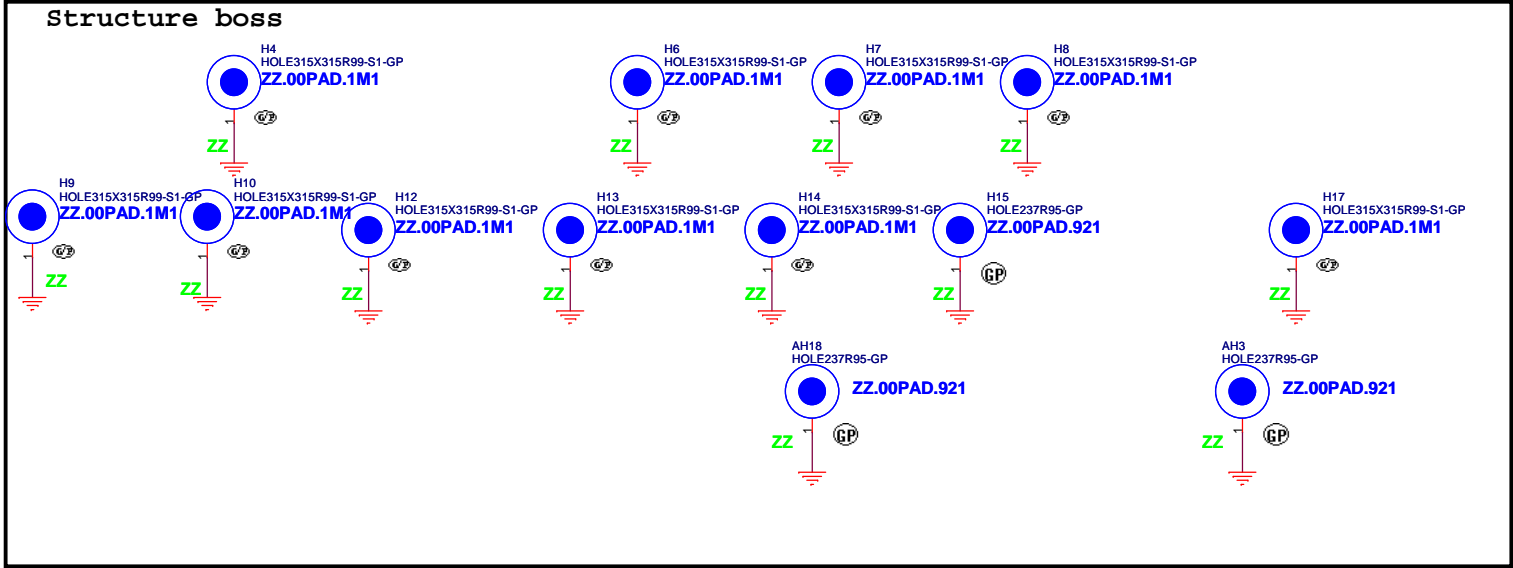
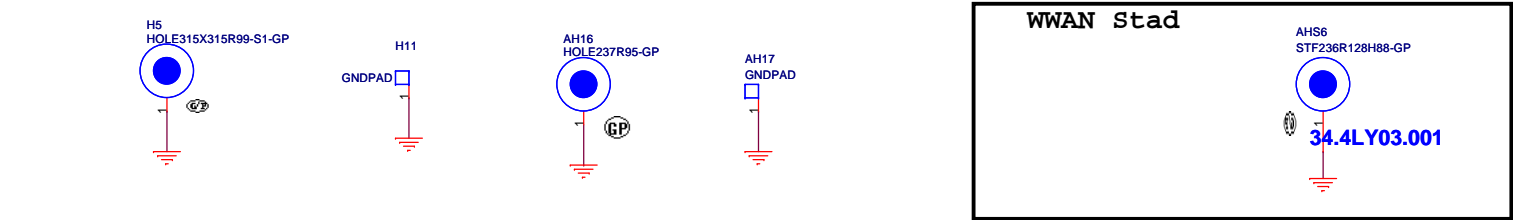
Date: Thursday, February 13, 2014

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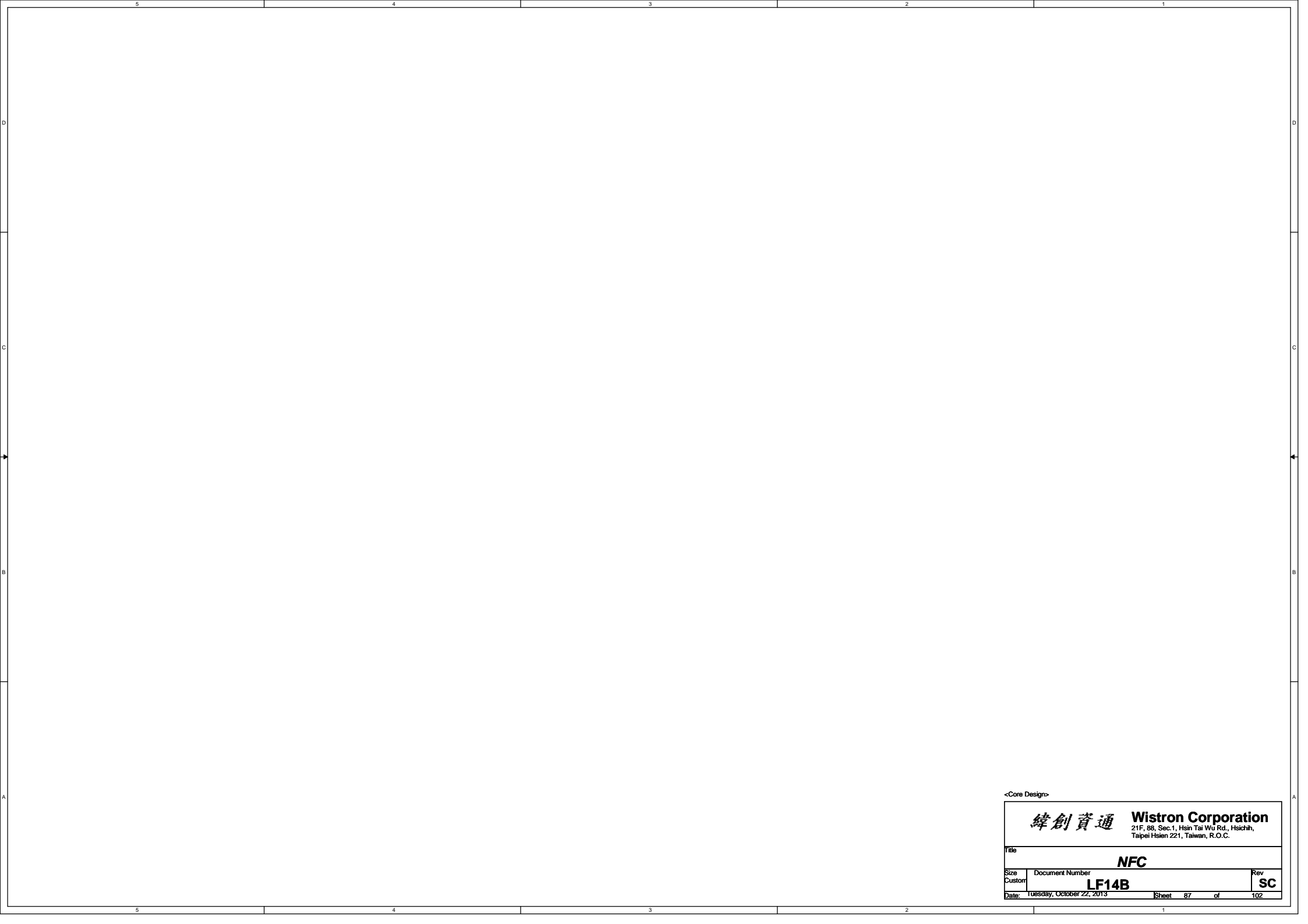
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Title			
Switchable GFX LCD(2/2)			
Size	Document Number		Rev
A4	LF14B		SA
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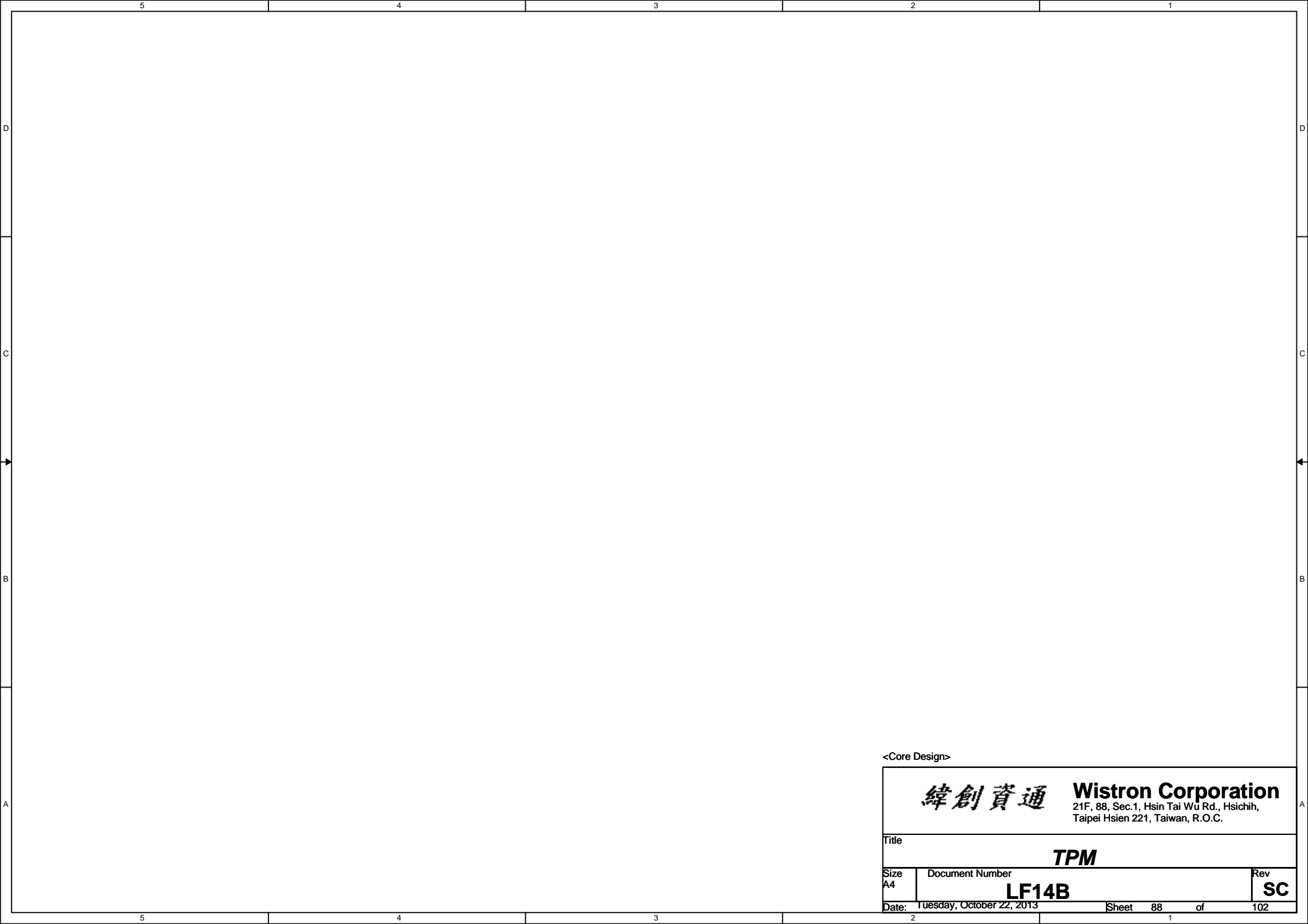
CPU Stad

VGA Stad



<Core Design>

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Title			
NFC			
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Title

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Size A4	Document Number LF14B	Rev SC
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SSID = Finger Print

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Size
A4

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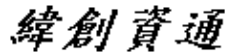
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SSID = Express Card

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SSID = Smart Card

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SSID = Docking

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SSID = Intel LAN

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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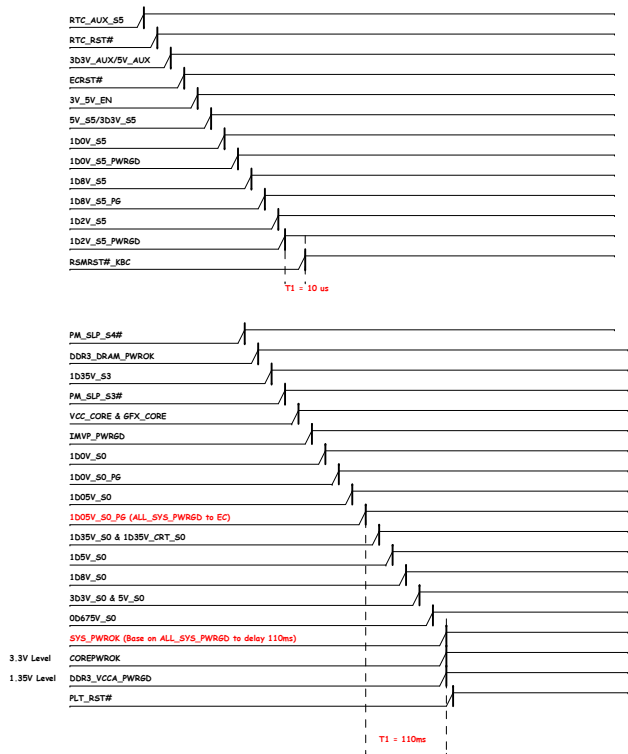
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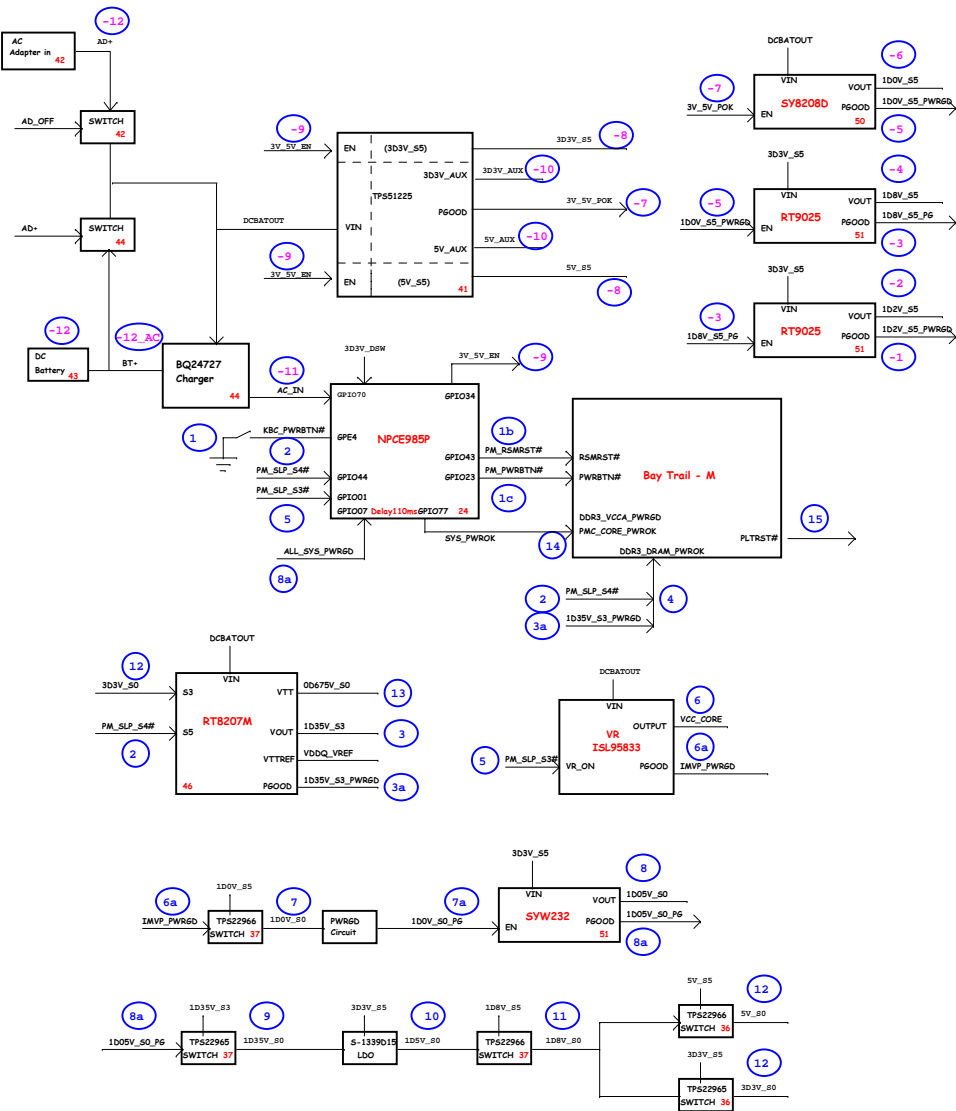
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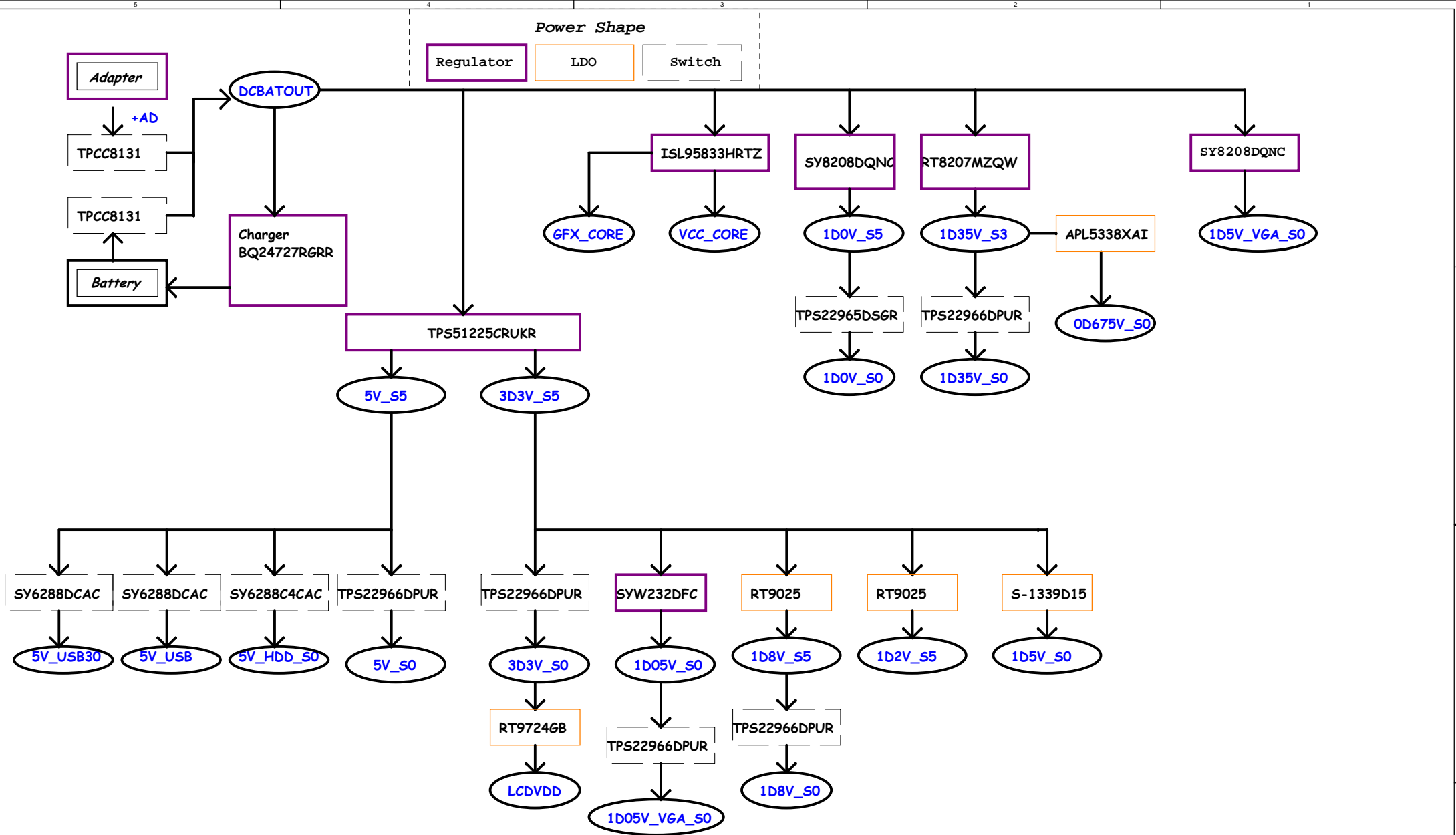
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Intel-Power Up Sequence with non-S0ix



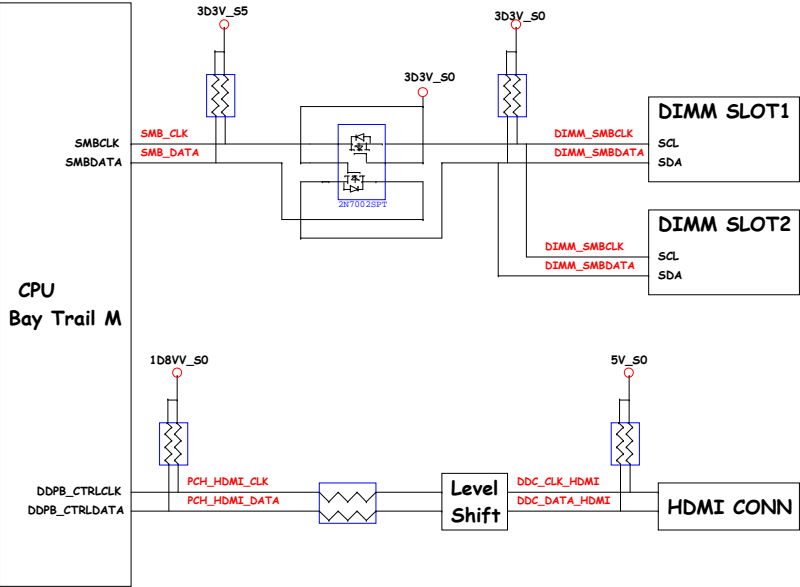
Bay Trail - M POWER UP SEQUENCE DIAGRAM



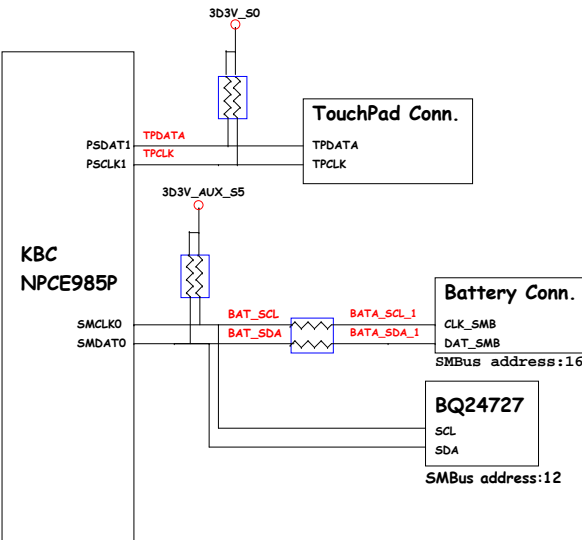


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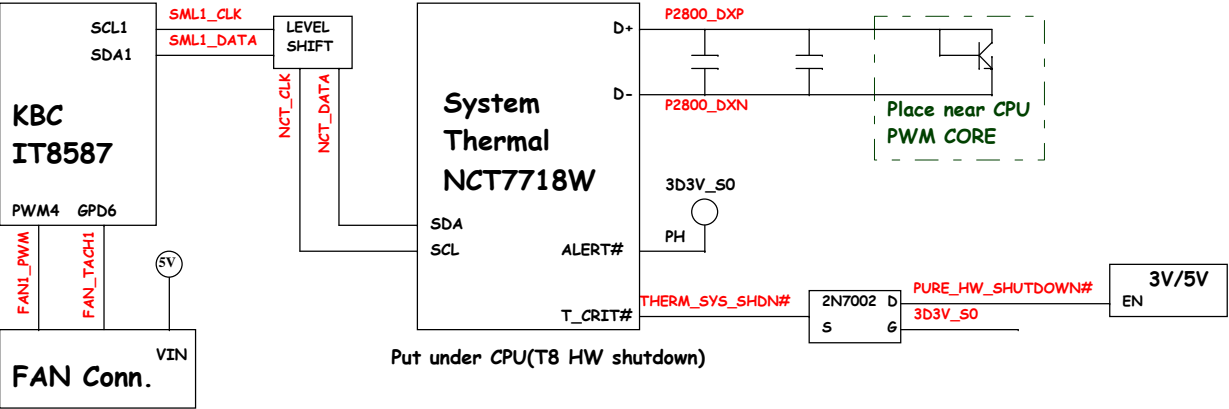
PCH SMBus Block Diagram



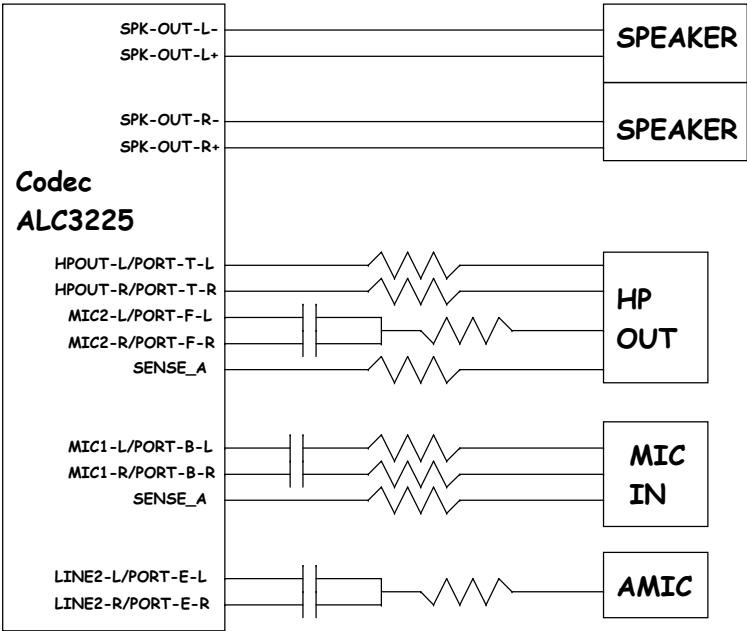
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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